DATA SHEET

TDA4867J
Full bridge current driven vertical deflection booster

Preliminary specification

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Philips
Semiconductors

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Full bridge current driven vertical deflection booster

TDA4867J

FEATURES

- Fully integrated, few external components
- Maximum 2.5 A (p-p) deflection current
- No additional components in combination with the deflection controller family TDA485x and SAA4856
- Pre-amplifier with differential high CMRR current mode inputs
- Low offsets
- High linear sawtooth signal amplification
- High efficient DC-coupled vertical output bridge circuit
- High deflection frequency up to 200 Hz
- Power supply and flyback supply voltage independent adjustable to optimize power consumption and flyback time
- Excellent transition behaviour during flyback
- Guard circuit for screen protection
- Power save mode controlled by input pins (in combination with SAA4856 only) or guard pin.

GENERAL DESCRIPTION

The TDA4867J is a power booster for use in colour vertical deflection systems for frame frequencies of 50 to 200 Hz. The circuit provides a high CMRR current driven differential input. Due to the bridge configuration of the two output stages DC-coupling of the deflection coil is achieved. In conjunction with the deflection controller family TDA485x and SAA4856 the ICs offer an extremely advanced system solution.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC supplies; note 1						
V_P	supply voltage		8.2	–	25	V
V_{FB}	flyback supply voltage	note 2	V_P + 6	–	60	V
$I_{q(VFB)}$	quiescent flyback current	no load; no signal	–	2.5	4	mA
Vertical circuit						
$I_{defl(p-p)}$	deflection current on pins OUTB and OUTA (peak-to-peak value)		0.6	–	2.5	A
$I_{i(dif)}$	differential input current	note 3	–	±500	±600	μA
Flyback generator						
$I_{FB(p-p)}$	maximum current during flyback on pin V_{FB} (peak-to-peak value)		–	–	2.5	A
Guard circuit; note 1						
V_{GUARD}	guard voltage	guard on	5.5	6.2	–	V

Notes

1. Voltages refer to pin GND.
2. If V_{FB} is between 40 and 60 V a decoupling capacitor C_{FB} = 22 μF (between pin V_{FB} and pin GND) and a resistor R_{FB} = 100 Ω (between pin V_{FB} and flyback supply voltage) are required (see Fig.6).
3. Differential input current $I_{i(dif)} = I_{INP} - I_{INN}$.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA4867J	DBS9P	plastic DIL-bent-SIL power package; 9 leads (lead length 12/11 mm); exposed die pad	SOT523-1

BLOCK DIAGRAM

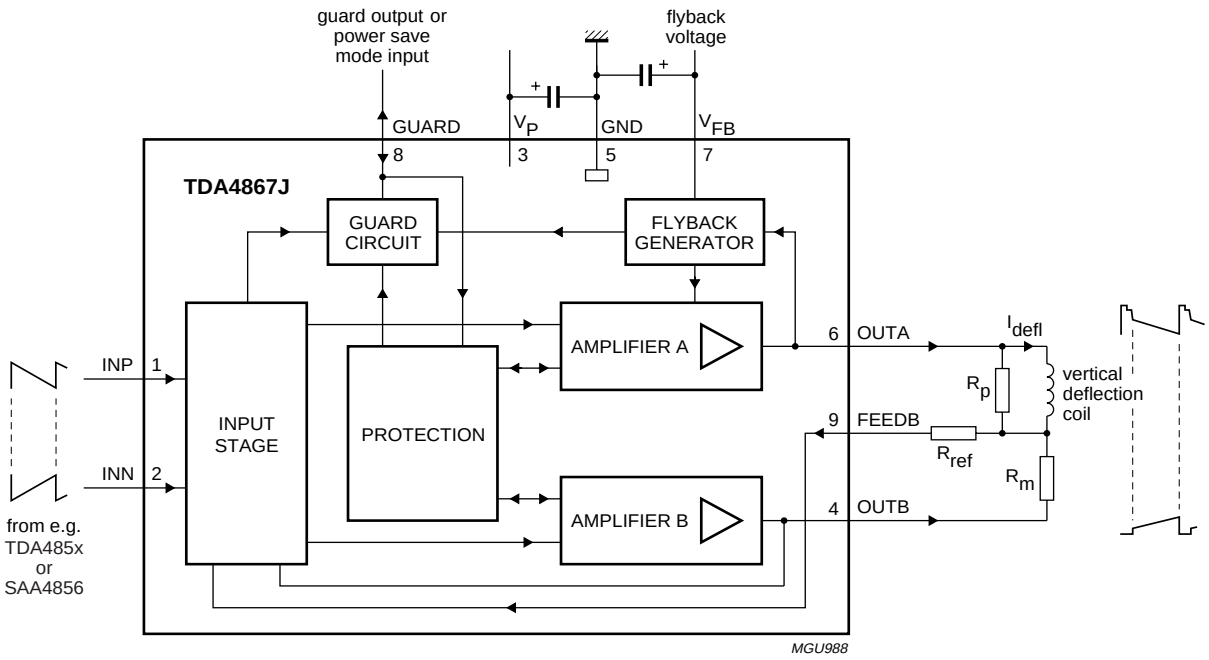


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
INP	1	non-inverted input
INN	2	inverted input
V_P	3	supply voltage
OUTB	4	output B
GND	5	ground
OUTA	6	output A
V_{FB}	7	flyback supply voltage
GUARD	8	guard output or power save mode input
FEEDB	9	feedback input

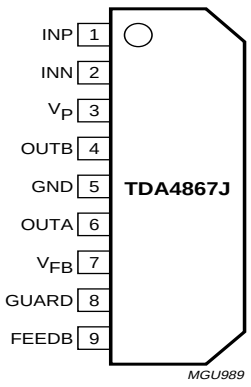


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA4867J consists of a differential input stage, two output stages, a flyback generator, a protection circuit for the output stages and a guard circuit.

Differential input stage

The differential input stage has a high CMRR differential current mode input (pin INP and pin INN) that results in a high electromagnetic immunity and is especially suitable for driver units with differential (e.g. TDA485x or SAA4856) and single-ended current signals.

The differential input stage delivers the driver signals for the output stages.

In combination with the SAA4856 the power save mode can be achieved via the input pins without additional components.

Output stages

The two output stages are current driven in opposite phase and operate in combination with the deflection coil in a full bridge configuration. Therefore, the TDA4867J requires no external coupling capacitor and operates with one supply voltage (V_P) and a separate adjustable flyback supply voltage (V_{FB}) only. The deflection current through the coil (I_{defl}) is measured with the resistor R_m which produces a voltage drop: $U_{rm} \approx R_m \times I_{defl}$. At pin FEEDB a part of I_{defl} is fed back to the input stage. The feedback input has a current input characteristic which holds the differential voltage between pin FEEDB and pin OUTB on zero.

Therefore the feedback current (I_{FEEDB}) through R_{ref} is:

$$I_{FEEDB} \approx \frac{R_m}{R_{ref}} \times I_{defl}$$

The input stage directly compares the driver currents into pins INP and INN with the half of the feedback current (I_{FEEDB}). Any difference of this comparison leads to a more or less driver current for the output stages. The relation between the deflection current and the differential input current ($I_{i(dif)} = I_{INP} - I_{INN}$) is:

$$I_{i(dif)} = 2 \times I_{FEEDB} \approx \frac{R_m}{R_{ref}} \times I_{defl} \times 2 \text{ or:}$$

$$I_{defl} \approx I_{i(dif)} \times \frac{R_{ref}}{2 \times R_m}$$

The deflection current can be adjusted up to ±1.25 A by varying R_{ref} when R_m is fixed to 1 Ω.

Flyback generator

The flyback generator supplies the output stage A during flyback. This makes it possible to optimize power consumption (supply voltage V_P) and flyback time (flyback voltage V_{FB}) separately. Due to the absence of a decoupling capacitor the flyback voltage is fully available.

In parallel with the deflection yoke and the damping resistor (R_p) an additional capacitor (C_{SP}) and a series resistor (R_{SP}) have to be used. The flyback time can be optimized depending on the value of C_{SP}.

Protection

The output stages are protected against:

- Thermal overshoot in normal operation
- Short-circuit of the coil (pins OUTB and OUTA).

Guard circuit

The internal guard circuit provides a blanking signal for the CRT. The guard signal is active HIGH:

- At thermal overshoot
- During flyback
- When missing flyback supply voltage
- When power supply voltage too low, $V_P < V_{P(min)}$.

The internal guard circuit will not be activated, if the input signals on pins INP and INN delivered from the driver circuit are out of range or at short-circuit of the coil (pins OUTB and OUTA).

For this reason an external guard circuit can be applied to detect failures of the deflection (see Fig.5). This circuit will be activated when flyback pulses are missing, which is the indication of any abnormal operation.

The guard output pin can be used as input for the power save mode. A current or a voltage has to be applied to the pin. In this case the output stages are switched off completely.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages referenced to ground (pin GND); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_P	supply voltage		0	30	V
V_{FB}	flyback supply voltage		0	60	V
I_{FB}	flyback supply current		0	±1.8	A
V_{INP}, V_{INN}	input voltage		0	5	V
I_{INP}, I_{INN}	input current		0	±5	mA
V_{OUTB}	output voltage on pin OUTB		0	V_P	V
V_{OUTA}	output voltage on pin OUTA		0	V_{FB}	V
I_{OUTB}, I_{OUTA}	output current	note 1	0	±1.6	A
V_{FEEDB}	feedback voltage		0	V_P	V
I_{FEEDB}	feedback current		0	±5	mA
V_{GUARD}	guard voltage		0	10	V
I_{GUARD}	guard current		0	±5	mA
T_{stg}	storage temperature		–20	+150	°C
T_{amb}	ambient temperature		–20	+75	°C
T_j	junction temperature	note 2	–20	+150	°C
V_{esd}	electrostatic discharge voltage	note 3	–4000	+4000	V
		note 4	–250	+250	V

Notes

1. Maximum output currents I_{OUTB} and I_{OUTA} are limited by current protection.
2. Internally limited by thermal protection; will be activated for $T_j \geq 150$ °C.
3. Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor.
4. Machine model: equivalent to discharging a 200 pF capacitor through a 0.75 μH inductance.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	note 1	4	K/W

Note

1. To minimize the thermal resistance from mounting base to heatsink [$R_{th(mb-h)}$] follow the recommended mounting instruction: screw mounting preferred; torque = 40 Ncm; use heatsink compound; isolation plate increases $R_{th(mb-h)}$.

CHARACTERISTICS

V_P = 12 V; T_{amb} = 25 °C; V_{FB} = 40 V; voltages referenced to ground (pin GND); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC supplies (pins V_P and V_{FB})						
V_P	supply voltage		8.2	–	25	V
V_{FB}	flyback supply voltage	note 1	V_P + 6	–	60	V
$I_{q(FB)}$	quiescent flyback current	no load; no signal	–	2.5	4	mA
$I_{q(P)}$	quiescent supply current	I_{defl} = 0	–	80	130	mA
Input stage (pins INP, INN and FEEDB)						
$I_{i(dif)}$	differential input current	note 2	–	±500	±600	µA
$I_{i(dif)(offset)}$	differential input offset current [$I_{i(dif)(offset)} = I_{INP} - I_{INN}$]	I_{defl} = 0; R_{ref} = 3 kΩ; R_m = 1 Ω	0	–	±20	µA
I_{INP}, I_{INN}	single-ended input current		0	±300	±600	µA
$V_{clamp(INP)}$	input clamp voltage on pin INP	$I_{INP} = I_{INN}$ = 0; note 3	2.7	3.0	3.3	V
$V_{clamp(INN)}$	input clamp voltage on pin INN	$I_{INP} = I_{INN}$ = 0; note 3	2.7	3.0	3.3	V
I_{FEEDB}	feedback current		–	±250	±300	µA
V_{FEEDB}	feedback voltage		1	–	V_P – 1	V
Output stages (pins OUTA and OUTB)						
$I_{defl(p-p)}$	deflection current (peak-to-peak value)		0.6	–	2.5	A
I_{OUTA}, I_{OUTB}	output current		±0.3	–	±1.25	A
$V_{sat(OUTA-GND)}$	saturation voltage pin OUTA to pin GND	I_{OUTA} = 0.7 A	–	1.1	1.3	V
		I_{OUTA} = 1.25 A; note 4	–	1.6	1.8	V
$V_{sat(VP-OUTA)}$	saturation voltage pin V_P to pin OUTA	I_{OUTA} = 0.7 A	–	2.1	2.7	V
		I_{OUTA} = 1.25 A; note 4	–	2.8	3.4	V
$V_{sat(OUTB-GND)}$	saturation voltage pin OUTB to pin GND	I_{OUTB} = 0.7 A	–	1.1	1.3	V
		I_{OUTB} = 1.25 A; note 4	–	1.6	1.8	V
$V_{sat(VP-OUTB)}$	saturation voltage pin V_P to pin OUTB	I_{OUTB} = 0.7 A	–	1.0	1.4	V
		I_{OUTB} = 1.25 A; note 4	–	1.6	2.0	V
LE	linearity error	I_{defl} = ±0.7 A; note 5	–	–	2	%
V_{OUTA}, V_{OUTB}	DC output voltage	$I_{i(dif)}$ = 0; closed loop	5.1	5.7	6.3	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Flyback generator						
$I_{FB(p-p)}$	maximum current during flyback on pin V_{FB} (peak-to-peak value)		–	–	2.5	A
$V_{FB-OUTA}$	voltage drop during flyback between pin V_{FB} and pin OUTA	reverse				
		I_{defl} = –0.7 A	–	–2.6	–3	V
		I_{defl} = –1.25 A	–	–3.1	–3.9	V
		forward				
		I_{defl} = 0.7 A	–	5.2	6.1	V
		I_{defl} = 1.25 A	–	5.7	6.9	V
$V_{th(OUTA)}$	switch-on threshold voltage on pin OUTA		V_P – 1	–	V_P + 1	V
Guard circuit (pin GUARD)						
V_{GUARD}	output voltage	guard on; I_{GUARD} = –5 mA	5	6	–	V
		guard off; I_{GUARD} = 0	–	–	0.4	V
I_{GUARD}	output current	guard on; V_{GUARD} > 5 V	–5	–	–	mA
V_{ext}	external voltage	for guard function	0	–	6.5	V
		for power save mode; I_{GUARD} = 0.5 mA	8.2	–	9.5	V

Notes

1. If V_{FB} is between 40 and 60 V a decoupling capacitor C_{FB} = 22 µF (between pin V_{FB} and pin GND) and a resistor R_{FB} = 100 Ω (between pin V_{FB} and flyback supply voltage) are required (see Fig.6).
2. Differential input current $I_{i(dif)} = I_{INP} - I_{INN}$.
3. Input resistance is 500 Ω.
4. Required V_P depends on the impedance of the deflection yoke.
5. Deviation of the output slope at a constant input slope.

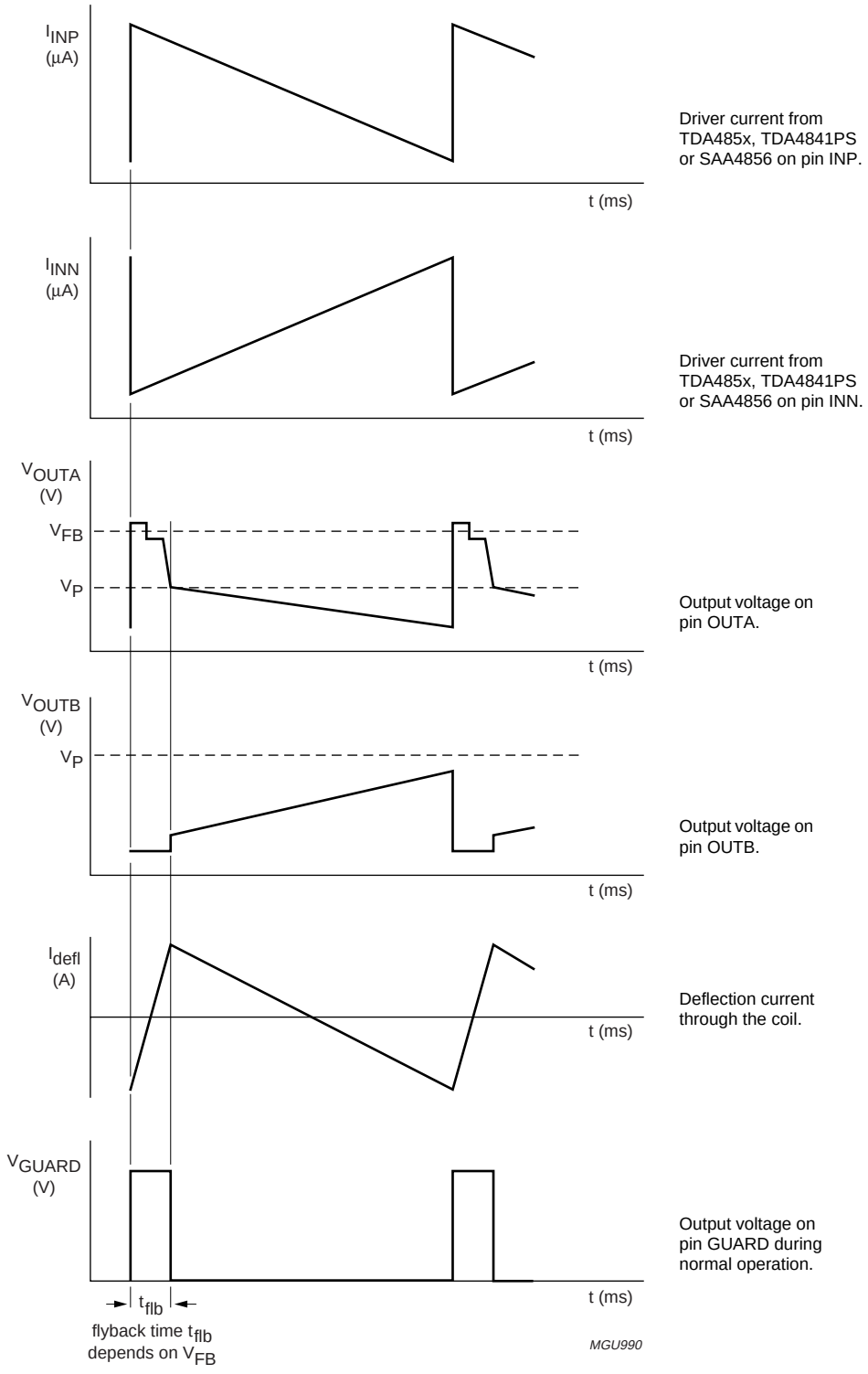


Fig.3 Timing diagram.

INTERNAL PIN CONFIGURATION

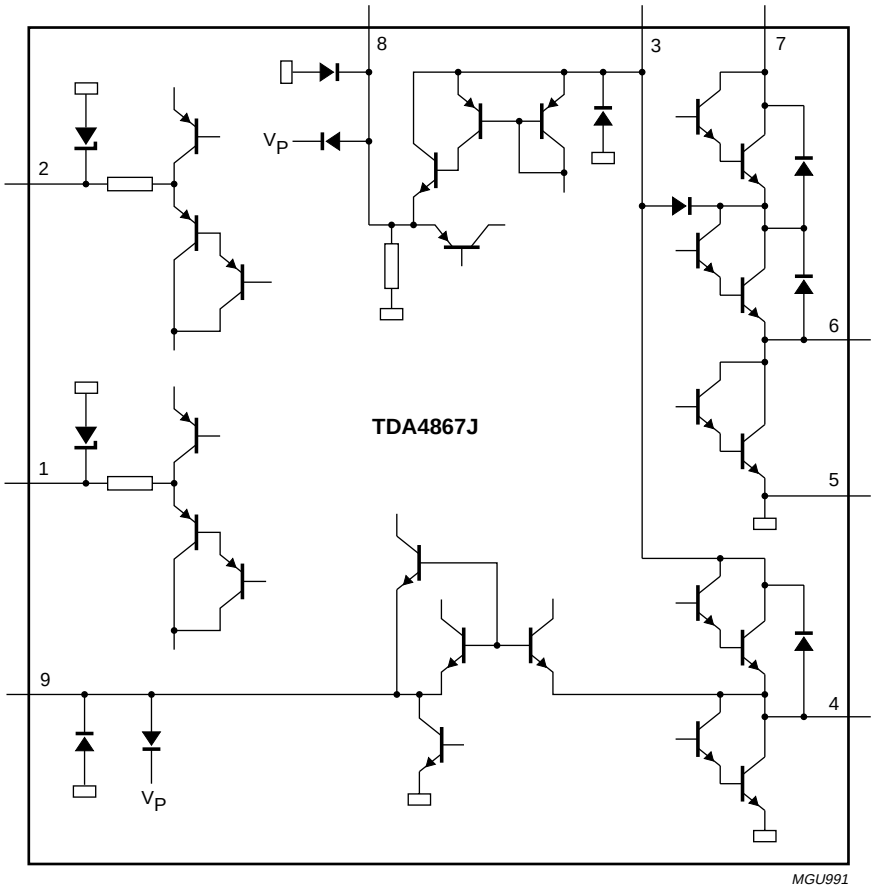


Fig.4 Internal circuits.

APPLICATION INFORMATION

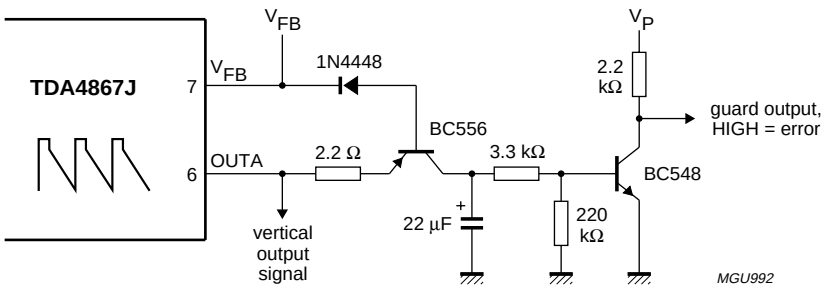
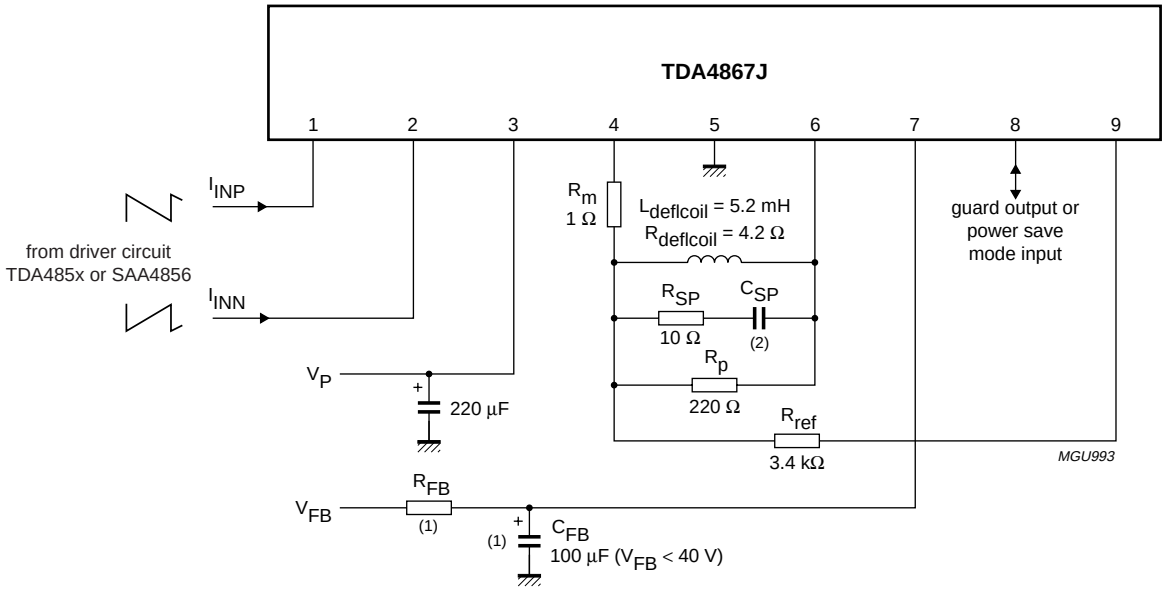


Fig.5 Application circuit for external guard signal generation.



(1) If V_{FB} is between 40 and 60 V a resistor R_{FB} = 100 Ω and a capacitor C_{FB} = 22 µF are required.

(2) The value of C_{SP} is application dependent, but 10 nF minimum is required.

Fig.6 Application diagram with driver circuit TDA485x or SAA4856.

Example

Table 1 Values given from application diagram Fig.6

SYMBOL	VALUE	UNIT
I_{defl}	0.71	A
$L_{deflcoil}$	5.2	mH
$R_{deflcoil}$	5.4 [= 4.2 + 7% + $\Delta R(\vartheta)$]	Ω
R_m	1 (+1%)	Ω
R_p	220	Ω
R_{ref}	3.4	kΩ
V_{FB}	40	V
T_{amb}	50	°C
$T_{deflcoil}$	75	°C
$R_{th(j-mb)}$	4	K/W
$R_{th(mb-amb)}$(1)	6	K/W

Note

1. Use heatsink compound.

Table 2 Calculated values

SYMBOL	VALUE	UNIT
V_P	8.5	V
t_{flb}	≈200	µs
P_{tot}	3.4	W
P_{defl}	0.9	W
P_{IC}	2.5	W
$R_{th(tot)}$	10	K/W
$T_{j(max)}$(1)	75	°C

Note

1. $T_{j(max)} = P_{IC} \times [R_{th(j-mb)} + R_{th(mb-amb)}] + T_{amb}$.

Calculation formulae for supply voltage:

$V_{b1} = V_{sat(VP-OUTA)} + R_{deflcoil} \times I_{defl} - U'_L + R_m \times I_{defl} + V_{sat(OUTB-GND)}$

$V_{b2} = V_{sat(OUTA-GND)} + R_{deflcoil} \times I_{defl} + U'_L + R_m \times I_{defl} + V_{sat(VP-OUTB)}$

for $V_{b1} > V_{b2}$: $V_P = V_{b1}$

for $V_{b2} > V_{b1}$: $V_P = V_{b2}$

where:

$U'_L = L_{deflcoil} \times 2 \times I_{defl} \times f_v$

f_v = vertical deflection frequency.

Calculation formulae for power consumption:

$$P_{IC} = P_{tot} - P_{defl}$$

$$P_{tot} = V_P \times \frac{I_{defl}}{2} + V_P \times 0.02\ A + 0.1\ W + V_{FB} \times I_{FB}$$

$$P_{defl} = \frac{1}{3} \times (R_{deflcoil} + R_m) \times I_{defl}^2$$

where:

P_{IC} = power dissipation of the TDA4867J

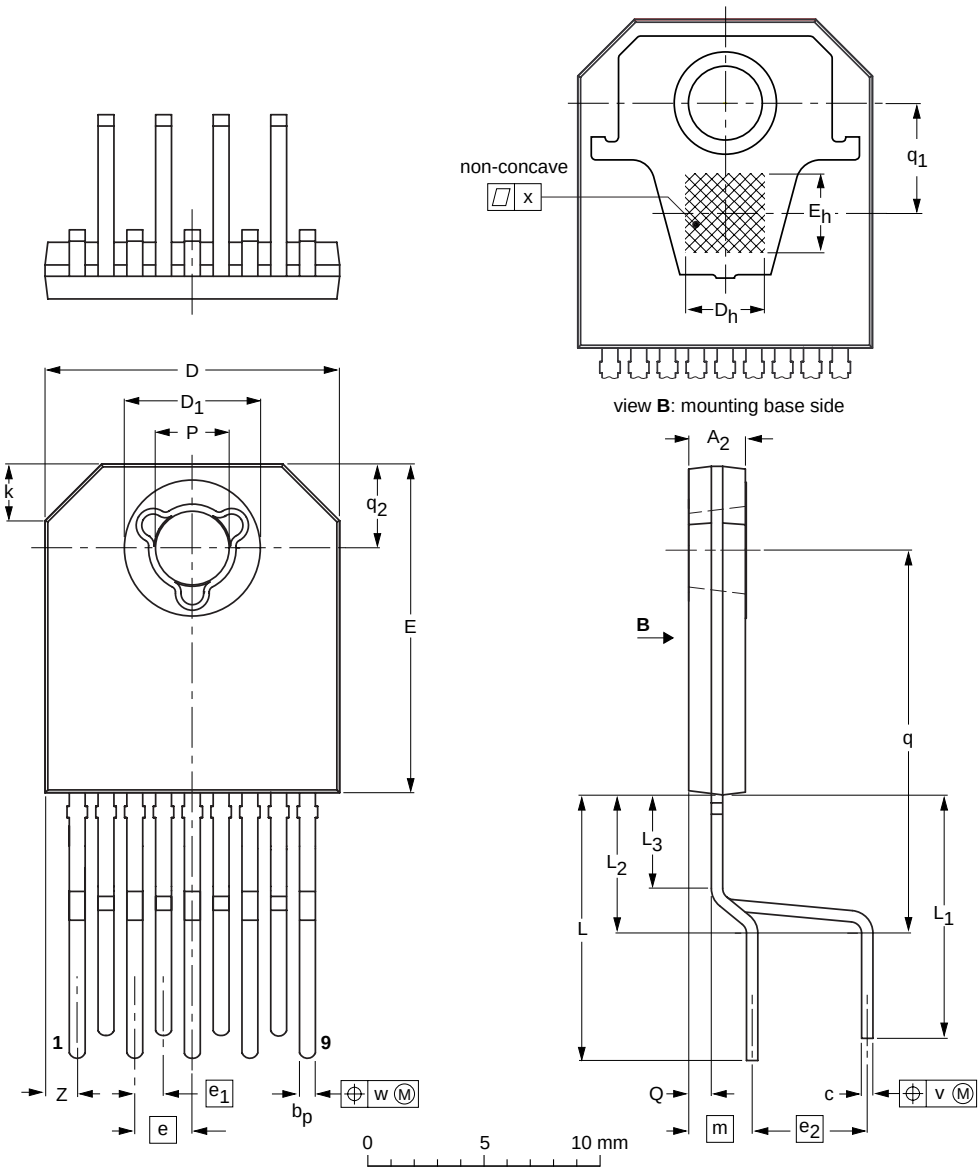
P_{tot} = total power dissipation

P_{defl} = power dissipation of the deflection coil.

Calculation formulae for flyback time (t_{flb}): $t_{flb} \approx \frac{L_{deflcoil}}{R_{deflcoil} + R_m} \times \ln\left(\frac{V_{FB} + (R_{deflcoil} + R_m) \times I_{defl}}{V_{FB} - (R_{deflcoil} + R_m) \times I_{defl}}\right)$

PACKAGE OUTLINE

DBS9P: plastic DIL-bent-SIL power package; 9 leads (lead length 12/11 mm); exposed die pad **SOT523-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A_2^{(2)}$	b_p	c	$D^{(1)}$	$D_1^{(2)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	k	L	L_1	L_2	L_3	m	P	Q	q	q_1	q_2	v	w	x	$Z^{(1)}$
mm	2.7 2.3	0.80 0.65	0.58 0.48	13.2 12.8	6.2 5.8	3.5	14.7 14.3	3.5	2.54	1.27	5.08	3.0 2.0	12.4 11.0	11.4 10.0	6.7 5.5	4.5 3.7	2.8	3.4 3.1	1.15 0.85	17.5 16.3	4.85	3.8 3.6	0.8	0.3	0.02	1.65 1.10

Notes

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.
2. Plastic surface within circle area D_1 may protrude 0.04 mm maximum.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT523-1						~~98-11-12~~ 00-07-03

SOLDERING

Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

Soldering by dipping or by solder wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Suitability of through-hole mount IC packages for dipping and wave soldering methods

PACKAGE	SOLDERING METHOD	
	DIPPING	WAVE
DBS, DIP, HDIP, SDIP, SIL	suitable	suitable[1]

Note

1. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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