TEXAS INSTRUMENTS

TAS5508A

8 Channel Digital Audio PWM Processor



Data Manual

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DAV–Digital Audio/Speaker

SLES119

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1 Introduction

The TAS5508A is an eight channel digital pulse width modulator (PWM) that provides both advanced performance and a high level of system integration. The TAS5508A is designed to interface seamlessly with most audio digital signal processors. The TAS5508A automatically adjusts control configurations in response to clock and data rate changes and idle conditions. This enables the TAS5508A to provide an easy to use control interface with relaxed timing requirements.

The TAS5508A can drive eight channels of H-bridge power stages. Texas Instruments H-bridge parts TAS5111, TAS5112, or TAS5182 + FETs are designed to work seamlessly with the TAS5508A. The TAS5508A supports both single-ended or bridge tied load configurations. The TAS5508A also provides a high performance differential output to drive an external differential input analog headphone amplifier (such as the TPA112).

The TAS5508A's uses an AD modulation operating at a 384-kHz switching rate for 48-, 96-, and 192-kHz data. The 8x over sampling combined with the 5th order noise shaper provides a broad flat noise floor and excellent dynamic range from 20 Hz to 20 kHz.

The TAS5508A is clock slave only device. The TAS5508A receives MCLK, SCLK and LRCLK from other system components. The TAS5508A accepts master clock rates of 128, 192, 256, 384, 512, and 768 Fs. The TAS5508A accepts a 64-Fs bit clock.

The TAS5508A allows for extending the dynamic range by providing a power supply volume control (PSVC) output signal.

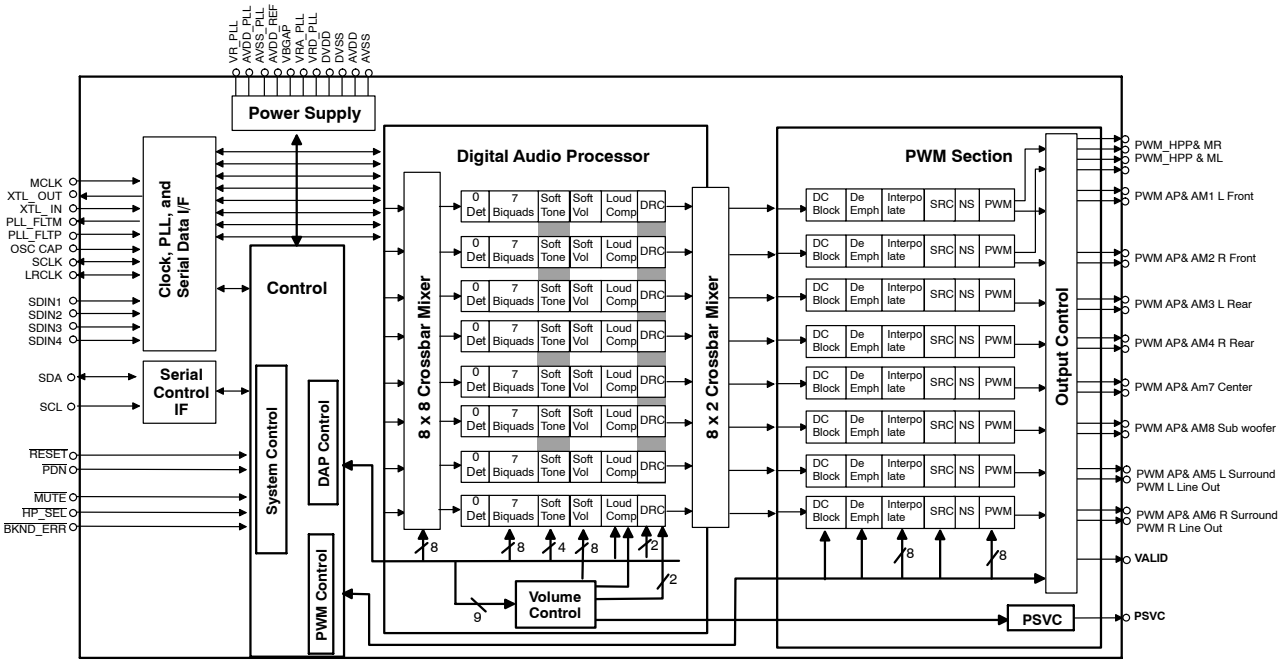


Figure 1–1. TAS5508A Functional Structure

1.1 TAS5508A System Diagrams

Typical applications for the TAS5508A are 6- to 8-channel audio systems such as DVD receiver or AV receiver. Figure 1–2 shows the basic system diagram of the DVD receiver.

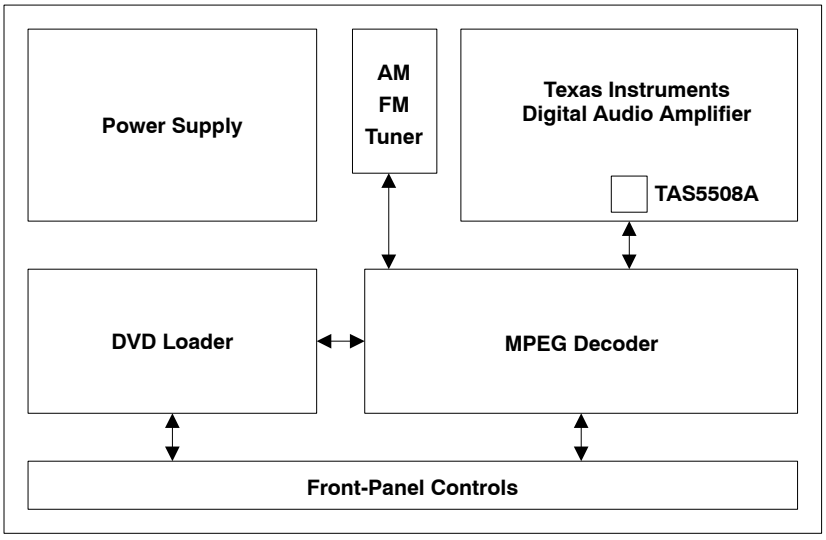


Figure 1–2. Typical TAS5508A Application (DVD Receiver)

Figure 1–3 shows the recommended channel configuration when using the TAS5508A with the TAS5121 power stage. Note that each channel is normally dedicated to a particular function.

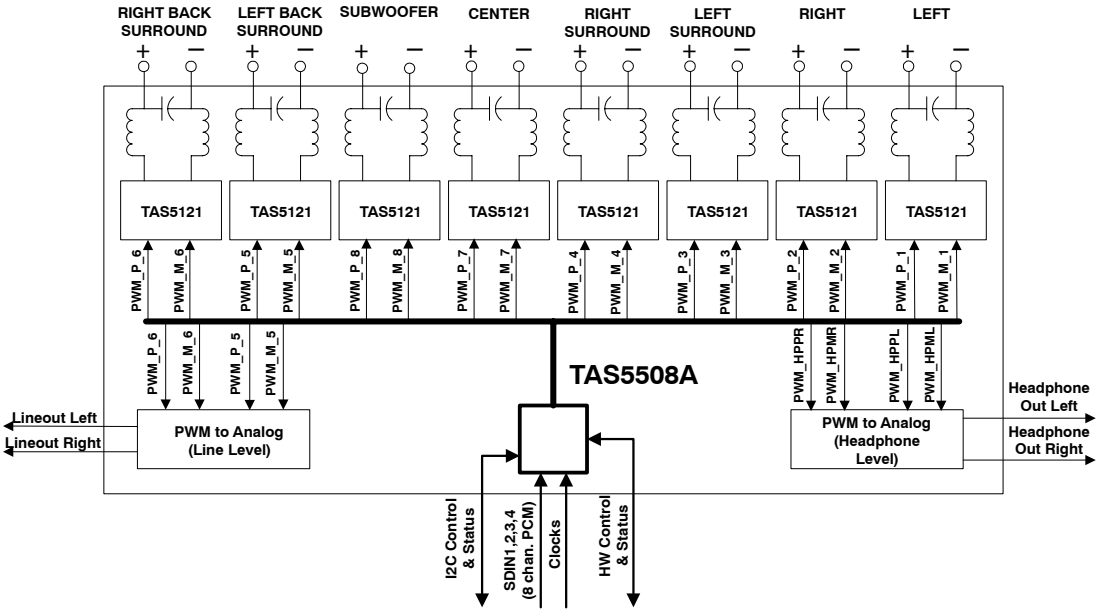


Figure 1–3. Recommended TAS5508A + TAS5121 Channel Configuration

1.2 TAS5508A Features

1.2.1 Audio Input / Output

- Automatic Master Clock Rate and Data Sample Rate Detection
- Eight Serial Audio Input Channels
- Eight PWM Audio Output Channels Configurable as Six Channels With Stereo Line Out or Eight Channels
- Line Output is a PWM Output to Drive an External Differential Input Operational Amplifier
- Headphone PWM Output to Drive an External Differential Amplifier Like the TPA112
- PWM Outputs Support Single Ended and Bridge Tied Loads
- 32-, 38-, 44.1-, 48-, 88.2-, 96-, 176.4-, and 192-kHz Sampling Rates
- Data Formats: 16-, 20-, or 24-bit input Data Left, Right and I^2S,
- 64 x Fs Bit Clock Rate
- 128, 192, 256, 384, 512, and 768 x Fs Master Clock Rates (Up to a Maximum of 50 MHz)

1.2.2 Audio Processing

- 48-Bit Processing Architecture With 76 bits of Precision for Most Audio Processing Features
- Volume Control Range +36 dB to – 127 dB
  - Master Volume Control Range of +18 dB to –100 dB
  - Eight Individual Channel Volume Control Range of +18-dB to –127-dB
- Programmable Soft Volume and Mute Update Rates
- Four Bass and Treble Tone Controls with ±18-dB Range, Selectable Corner Frequencies, and 2^{nd} Order Slopes
  - L, R, and C
  - LS, RS
  - LR, RR
  - Sub
- Configurable Loudness Compensation
- Two Dynamic Range Compressors With Two Thresholds, Two Offsets, and Three Slopes
- Seven Bi-quads Per Channel
- Full 8x8 Input Crossbar Mixer. Each Signal Processing Channel Input Can Be Any Ratio of the Eight Input Channels
- 8x2 Output Mixer – Channels 1–6. Each Output Can Be Any Ratio of Any Two Signal Processed Channels
- 8x3 Output mixer – Channels 7 and 8. Each Output can be Any Ratio of Any Three Signal Processed Channels
- Three Coefficient Sets Stored on the Device Can be Selected Manually or Automatically (Based on Specific Data Rates)
- DC Blocking Filters
- Able to Support a Variety of Bass Management Algorithms

1.2.3 PWM Processing

- 32-Bit Processing PWM Architecture With 40 Bits of Precision
- 8x Oversampling With 5th Order Noise Shaping at 32 – 48 kHz, 4x Oversampling at 88.2 kHz, and 96 kHz and 2x Oversampling at 176.4 kHz and 192 kHz
- >102-dB Dynamic Range
- THD+N < 0.1%
- 20 – 20-kHz Flat Noise Floor for 44.1-, 48-, 88.2-, 96-, 176.4-, and 192-kHz Data Rates
- Digital De-emphasis for 32-, 44.1-, and 48-kHz Data Rates
- Flexible Automute Logic With Programmable Threshold and Duration for Noise Free Operation
- Intelligent AM Interference Avoidance System Provides Clear AM Reception
- Power Supply Volume Control (PSVC) Support for Enhanced Dynamic Range in High Performance Applications
- Adjustable Modulation Limit

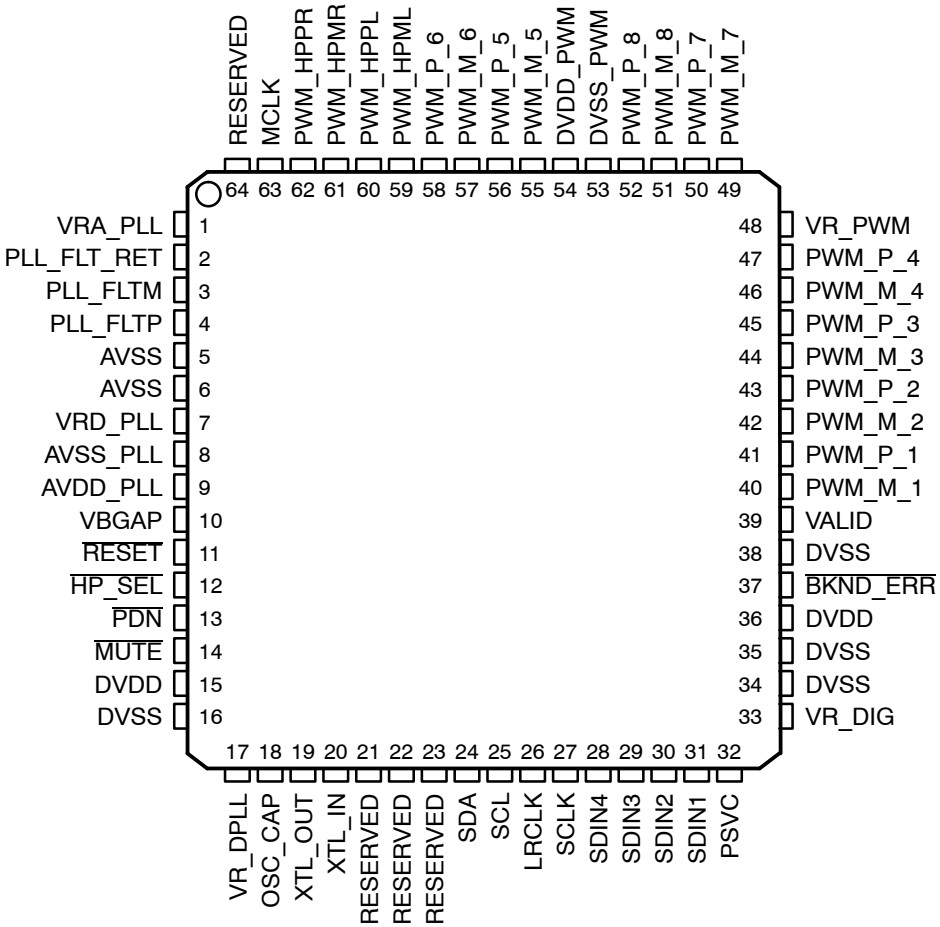
1.2.4 General Features

- Automated Operation With an Easy to Use Control Interface
- I^{2}C Serial Control Slave Interface
- Integrated AM Interference Avoidance Circuitry
- Single 3.3-V Power Supply
- 64-Pin TQFP Package
- 5-V Tolerant Inputs

1.3 Physical Characteristics

1.3.1 Terminal Assignments

TQFP PACKAGE
(TOP VIEW)



1.3.2 Ordering Information

T_A	PLASTIC 64-PIN PQFP (PN)
0°C to 70°C	TAS5508APAG

1.3.3 Terminal Descriptions

TERMINAL NO.	TERMINAL NAME	I/O	5-V TOLERANT	TERMINATION	DESCRIPTION
1	VRA_PLL				Voltage reference for PLL analog supply 1.8 V. A pin-out of the internally regulated 1.8-V power used by PLL logic. A 0.1-μF low ESR capacitor should be connected between this terminal and AVSS_PLL. This terminal must not be used to power external devices.
2	PLL_FLT_RET	AO			PLL external filter return
3	PLL_FLTM	AO			PLL negative input. Connected to PLL_FLT_RTN via an RC network
4	PLL_FLTP	AI			PLL positive input. Connected to PLL_FLT_RTN via an RC network
5	AVSS	P			Analog ground
6	AVSS	P			Analog ground

TERMINAL NO.	TERMINAL NAME	I/O	5-V TOLERANT	TERMINATION	DESCRIPTION
7	VRD_PLL	P			Voltage reference for PLL digital supply 1.8 V. A pin-out of the internally regulated 1.8-V power used by PLL logic. A 0.1-μF low ESR capacitor should be connected between this terminal and AVSS_PLL. This terminal must not be used to power external devices.
8	AVSS_PLL	P			Analog ground for PLL. This terminal should reference the same ground as power terminal DVSS, but to achieve low PLL jitter; ground noise at this terminal must be minimized. The availability of the AVSS terminal allows a designer to use optimizing techniques such as star ground connections, separate ground planes, or other quiet ground distribution techniques to achieve a quiet ground reference at this terminal.
9	AVDD_PLL	P			3.3-V analog power supply for PLL This terminal can be connected to the same power source used to drive power terminal DVDD, but to achieve low PLL jitter, this terminal should be bypassed to AVDD_PLL with a 0.1-μF low-ESR capacitor.
10	VBGAP	P			Band gap voltage reference. A pin-out of the internally regulated 1.2-V reference. Typically has a 1-nF low ESR capacitor between VBGAP and AVSS_PLL. This terminal must not be used to power external devices.
11	$\overline{\text{RESET}}$	DI	5 V	Pull up	System reset input, active low. A system reset is generated by applying a logic low to this terminal. $\overline{\text{RESET}}$ is an asynchronous control signal that restores the TAS5508A to its default conditions, sets the valid output low, and places the PWM in the hard mute (M) state. Master volume is immediately set to full attenuation. Upon the release of $\overline{\text{RESET}}$, if $\overline{\text{PDN}}$ is high, the system performs a 4–5 ms. device initialization and set the volume at mute.
12	$\overline{\text{HP_SEL}}$	DI	5 V	Pull up	Headphone in/out selector. When a logic low is applied, the headphone is selected (speakers are off). When a logic high is applied, speakers are selected – headphone is off.
13	$\overline{\text{PDN}}$	DI	5 V	Pull up	Power down, active low. PDN powers down all logic and stops all clocks whenever a logic low is applied. The internal parameters are preserved through a power down cycle, as long as a RESET is not active. The duration for system recovery from power down is 100 ms.
14	$\overline{\text{MUTE}}$	DI	5 V	Pull up	Soft mute of outputs, active low (Muted signal = a logic low, normal operation = a logic high) The mute control provides a noiseless volume ramp to silence. Releasing mute provides a noiseless ramp to previous volume.
15	DVDD	P			Digital power 3.3-V supply for digital core and most of I/O buffers
16	DVSS	P			Digital ground for digital core and most of I/O buffers
17	VR_DPLL	P			Voltage reference for digital PLL supply 1.8 V. A pin-out of the internally regulated 1.8-V power used by digital PLL logic. A 0.1–μF low ESR capacitor should be connected between this terminal and DVSS_CORE. This terminal must not be used to power external devices.
18	OSC_CAP	AO			Oscillator capacitor
19	XTL_OUT	AO			XTL_OUT and XTL_IN are the only LVCMOS terminals on the device. They provide a reference clock for the TAS5508A via use of an external fundamental mode crystal. XTL_OUT is the 1.8-V output drive to the crystal. See Note 4 for the recommended crystal type.
20	XTL_IN	AI			XTL_OUT and XTL_IN are the only LVCMOS terminals on the device. They provide a reference clock for the TAS5508A via use of an external fundamental mode crystal. XTL_IN is the 1.8-V input port for the oscillator circuit. See Note 4 for the recommended crystal type.
21	RESERVED				Connect to digital ground
22	RESERVED				Connect to digital ground
23	RESERVED				Connect to digital ground
24	SDA	DIO	5 V		I^2C serial control data interface input / output
25	SCL	DI	5 V		I^2C serial control clock input output
26	LRCLK	DI	5 V		Serial audio data left / right clock (sampling rate clock)
27	SCLK	DI	5 V		Serial audio data clock (shift clock) SCLKIN is the serial audio port (SAP) input data bit clock that is supplied to the serial bit clock to other I^2S bus.

TERMINAL NO.	TERMINAL NAME	I/O	5-V TOLERANT	TERMINATION	DESCRIPTION
28	SDIN4	DI	5 V	Pulldown	Serial audio data 4 input is one of the serial data input ports. SDIN4 supports four discrete (stereo) data formats and is capable of inputting data at 64 Fs.
29	SDIN3	DI	5 V	Pulldown	Serial audio data 3 input is one of the serial data input ports. SDIN3 supports four discrete (stereo) data formats and is capable of inputting data at 64 Fs.
30	SDIN2	DI	5 V	Pulldown	Serial audio data 2 input is one of the serial data input ports. SDIN2 supports four discrete (stereo) data formats and is capable of inputting data at 64 Fs.
31	SDIN1	DI	5 V	Pulldown	Serial audio data 1 input is one of the serial data input ports. SDIN1 supports four discrete (stereo) data formats and is capable of inputting data at 64 Fs.
32	PSVC	O			Power supply volume control PWM output
33	VR_DIG	P			Voltage reference for digital core supply 1.8 V. A pin-out of the internally regulated 1.8-V power used by digital core logic. A 0.47-μF low ESR capacitor should be connected between this terminal and DVSS. This terminal must not be used to power external devices
34	DVSS	P			Digital ground
35	DVSS	P			Digital ground
36	DVDD	P			3.3-V digital power supply
37	$\overline{\text{BKND_ERR}}$	DI		Pull up	Active low. A backend error sequence is generated by applying logic low to this terminal. The $\overline{\text{BKND_ERR}}$ results in all system parameters unaffected, while all H-bridge drive signals going to a hard mute (M) state.
38	DVSS	P			Digital ground
39	VALID	DO			Output indicating validity of PWM outputs active high
40	PWM_M_1	DO			PWM 1 output (differential –)
41	PWM_P_1	DO			PWM 1 output (differential +)
42	PWM_M_2	DO			PWM 2 output (differential –)
43	PWM_P_2	DO			PWM 2 output (differential +)
44	PWM_M_3	DO			PWM 3 output (differential –)
45	PWM_P_3	DO			PWM 3 output (differential +)
46	PWM_M_4	DO			PWM 4 output (differential –)
47	PWM_P_4	DO			PWM 4 output (differential +)
48	VR_PWM	P			Voltage reference for digital PWM core supply 1.8 V. A pin-out of the internally regulated 1.8-V power used by digital PWM core logic. A 0.1-μF low ESR capacitor should be connected between this terminal and DVSS_PWM. This terminal must not be used to power external devices.
49	PWM_M_7	DO			PWM 7 (Line out L) output (differential –)
50	PWM_P_7	DO			PWM 7 (Line out L) output (differential +)
51	PWM_M_8	DO			PWM 8 (Line out R) output (differential –)
52	PWM_P_8	DO			PWM 8 (Line out R) output (differential +)
53	DVSS_PWM	P			Digital ground for PWM
54	DVDD_PWM	P			3.3-V digital power supply for PWM
55	PWM_M_5	DO			PWM 5 output (differential –)
56	PWM_P_5	DO			PWM 5 output (differential +)
57	PWM_M_6	DO			PWM 6 output (differential –)
58	PWM_P_6	DO			PWM 6 output (differential +)
59	PWM_HPML	DO			PWM left channel headphone (differential –)
60	PWM_HPPL	DO			PWM left channel headphone (differential +)
61	PWM_HPMR	DO			PWM right channel headphone (differential –)
62	PWM_HPPR	DO			PWM right channel headphone (differential +)

TERMINAL NO.	TERMINAL NAME	I/O	5-V TOLERANT	TERMINATION	DESCRIPTION
63	MCLK	DI	5 V	Pulldown	MCLK is a 3.3-V clock master clock input. The input frequency of this clock can range from 4 MHz to 50 MHz.
64	RESERVED				Connect to digital ground

NOTES: 1. Type: A = analog; D = 3.3-V digital; P = power / ground / decoupling; I = input; O = output
2. All pullups are 20-μA weak pullups and all pulldowns are 20-μA weak pull downs. The pullups and pulldowns are included to assure proper input logic levels if the terminals are left unconnected (pullups => logic 1 input; pulldowns => logic 0 input). Devices that drive inputs with pull ups must be able to sink 20 μA, while maintaining a logic 0 drive level. Devices that drive inputs with pulldowns must be able to source 20 μA, while maintaining a logic '1' drive level.
3. If desired, low ESR capacitance values can be implemented by paralleling two or more ceramic capacitors of equal value. Paralleling capacitors of equal value provide an extended high frequency supply decoupling. This approach avoids the potential of producing parallel resonance circuits that have been observed when paralleling capacitors of different values.
4. 13.5-MHz crystal (HCM49)

1.4 TAS5508A Functional Description

Figure 1–4 shows the TAS5508A functional structure. The next sections describe the TAS5508A functional blocks:

- Power Supply
- Clock, PLL, and Serial Data Interface
- Serial Control Interface
- Device Control
- Digital Audio Processor (DAP)
- Pulse Width Modulation (PWM) Processor

1.4.1 Power Supply

The power supply section contains supply regulators that provide analog and digital regulated power for various sections of the TAS5508A. The analog supply supports the analog PLL, while digital supplies support the digital PLL, the digital audio processor (DAP), the pulse width modulator (PWM), and the output control (reclocker). The regulators can also be turned off when terminals $\overline{\text{RESET}}$ and $\overline{\text{PDN}}$ are both low.

1.4.2 Clock, PLL, and Serial Data Interface

The TAS5508A is a clock slave only device and it requires the use of an external 13.5 MHz crystal. It accepts MCLK, SCLK, and LRCLK as inputs only.

The TAS5508A uses the external crystal to provide a time base for:

- Continuous data and clock error detection and management
- Automatic data rate detection and configuration
- Automatic MCLK rate detection and configuration (automatic bank switching)
- Supporting I^2C operation/ communication while MCLK is absent

The TAS5508A automatically handles clock errors, data rate changes, and master clock frequency changes without requiring intervention from an external system controller. This feature significantly reduces system complexity and design.

1.4.2.1 Serial Audio Interface

The TAS5508A operates as a slave only / receive only serial data interface in all modes. The TAS5508A has four PCM serial data interfaces to permit eight channels of digital data to be received though the SDIN1, SDIN2, SDIN3, and SDIN4 inputs. The serial audio data is in MSB first, two's complement format.

The serial data input interface of the TAS5508A can be configured in right justified, I^{2}S, or left-justified modes. The serial data interface format is specified using the I^{2}C data interface control register. The supported formats and word lengths are shown in Table 1−1.

Table 1−1. Serial Data Formats

RECEIVE SERIAL DATA INTERFACE FORMAT	WORD LENGTHS
Right justified	16
Right justified	20
Right justified	24
I2S	16
I2S	20
I2S	24
Left Justified	16
Left Justified	20
Left Justified	24

Serial data is input on SDIN1, SDIN2, SDIN3, and SDIN4. The TAS5508A accepts 32-, 38-, 44.1-, 48-, 88.2-, 96-, 176.4-, and 192-kHz serial data in 16-, 20-, or 24-bit data in left, right, and I^{2}S serial data formats using a 64-Fs SCLK clock and a 128, 192, 256, 384, 512, or 768 x Fs MCLK rates (up to a maximum of 50 MHz). The parameters of this clock and serial data interface are I^{2}C configurable.

1.4.3 I^{2}C Serial Control Interface

The TAS5508A has an I^{2}C serial control slave interface (address 0x36) to receive commands from a system controller. The serial control interface supports both normal-speed (100 kHz) and high-speed (400 kHz) operations without wait states. Since the TAS5508A has a crystal time base, this interface operates even when MCLK is absent.

The serial control interface supports both single byte and multi-byte read / write operations for status registers and the general control registers associated with the PWM. However, for the DAP data processing registers, the serial control interface also supports multiple byte (4 byte) write operations.

The I^{2}C supports a special mode which permits I^{2}C write operations to be broken up into multiple data write operations that are multiples of 4 data bytes. These are 6 byte, 10 byte, 14 byte, 18 byte ... etc write operations that are composed of a device address, read/write bit, and subaddress and any multiple of 4 bytes of data. This permits the system to incrementally write large register values without blocking other I^{2}C transactions. In order to use this feature, the first chunk of data is written to the target I^{2}C address and each subsequent chunk of data is written to a special append register (0xFE) until all the data is written and a stop bit is sent. An incremental read operation is not supported.

1.4.4 Device Control

The TAS5508A control section provides the control and sequencing for the TAS5508A. The device control provides both high and low level control for the serial control interface, clock and serial data interfaces, digital audio processor, and pulse width modulator sections.

1.4.5 Digital Audio Processor (DAP)

The DAP arithmetic unit is used to implement all audio processing functions − soft volume, loudness compensation, bass and treble processing, dynamic range control, channel filtering, input and output mixing. Figure 1−6 shows the TAS5508A DAP architecture.

The DAP accepts 24-bit data signal from the serial data interface and outputs 32-bit data to the PWM section. The DAP supports two configurations, one for 32-kHz – 96-kHz data and one for 176.4-kHz to 192-kHz data.

1.4.5.1 TAS5508A Audio Processing Configurations

The 32 – 96 kHz configuration supports eight channels of data processing that can be configured as eight channels or six channels with two channels for separate stereo line outputs.

The 176.4 – 192 kHz configuration supports three channels of signal processing with five channels passed though (or derived from the three processed channels).

To efficiently support the processing requirements of both multi-channel 32 – 96-kHz data and the two channel 176.4 and 192-kHz data, the TAS5508A supports separate audio processing features for 32 –96-kHz data rates and for 176.4 and 192 kHz. See Table 2 for a summary of TAS5508A processing feature sets.

1.4.5.2 TAS5508A Audio Signal Processing Functions

The DAP provides 10 primary signal processing functions.

1. The data processing input has a full 8x8 input crossbar mixer. This enables each input to be any ratio of the eight input channels.
2. Two I^2C programmable threshold detectors in each channel support automute.
3. Seven biquads per channel
4. Four soft bass and treble tone controls with ±18 dB range, programmable corner frequencies, and 2nd order slopes. In 8-channel mode, bass and treble controls are normally configured as follows:
   - Bass and Treble 1: Channel 1 (Left), Channel 2 (Right), and Channel 7 (Center)
   - Bass and Treble 2: Channel 3 (Left Surround) and Channel 4 (Right Surround)
   - Bass and Treble 3: Channel 5 (Left Back Surround) and Channel 6 (Right Back Surround)
   - Bass and Treble 4: Channel 8 (Subwoofer)
5. Individual channel and master volume controls. Each control provides an adjustment range of +18 dB to –127 dB. This permits a total volume device control range of +36 dB to –127 dB plus mute. The master volume control can be configured to control six or eight channels. The DAP soft volume and mute update interval is I^2C programmable. The update is performed at a fixed rate regardless of the sample rate.
6. Programmable loudness compensation that is controlled via the combination of the master and individual volume settings.
7. Two dual-threshold dual-rate dynamic range compressors (DRCs). The volume gain values are provided used as input parameters using the maximum RMS (master volume x individual channel volume).
8. 8x2 output mixer (channels 1–6). Each output can be any ratio of any two signal processed channels.
9. 8x3 output mixer (channels 7 and 8). Each output can be any ratio of any three signal processed channels.
10. The DAP maintains three sets of coefficient banks that are used to maintain separate sets of sample rate dependent parameters for the biquad, tone controls, loudness, and DRC in RAM. These can be set to be automatically selected for one or more data sample rates or can be manually selected under I^2C program control. This feature enables coefficients for different sample rates to be stored in the TAS5508A and then select when needed.

Table 1–2. TAS5508A Audio Processing Feature Sets

FEATURE	32 – 96 kHz 8 CHANNEL FEATURE SET	32 – 96 kHz 6 + 2 LINE OUT FEATURE SET	176.4- AND 192-kHz FEATURE SET
Signal processing channels	8	6 + 2	3
Pass through channels	N/A		5
Master volume	1 for eight channels	1 for six channels	1 for three channels
Individual channel volume controls	8		3
Bass and treble tone controls	Four Bass and Treble tone controls with ±18 dB range, programmable corner frequencies, and 2nd order slopes L, R and C (Ch 1, 2, and 7) LS, RS (Ch 3 and 4) LBS, RBS (Ch 5 and 6) Sub (Ch 8)	Four Bass and Treble tone controls with ±18 dB range, programmable corner frequencies, and 2nd order slopes L, R and C (Ch 1, 2, and 7) LS, RS (Ch 3 and 4) Sub, (Ch 8) Line L and R (Ch 5 and 6)	Two Bass and Treble tone controls with ±18 dB range, programmable corner frequencies, and 2nd order slopes L and R (Ch 1 and 2) Sub (Ch 8)
Biquads	56		21
Dynamic range compressors	DRC1 for seven satellites and DRC2 for sub	DRC1 for five satellites and DRC2 for sub (Ch 5 and 6 Uncompressed)	DRC1 for two satellites and DRC2 for sub
Input output mapping/mixing	Each of the eight signal-processing channels input can be any ratio of the eight input channels. Each of the eight outputs can be any ratio of any two processed channels.		Each of the three signal-processing channels or the five pass-though channels inputs can be any ratio of the eight input channels. Each of the eight outputs can be any ratio of any of the three processed or five bypass channels.
DC blocking filters (Implemented in PWM Section)	Eight channels		
Digital de-emphasis (Implemented in PWM Section)	Eight channels for 32 kHz, 44.1 kHz, and 48 kHz	Six channels for 32 kHz, 44.1 kHz, and 48 kHz	N/A
Loudness	Eight channels	Six channels	Three channels
Number of coefficient sets stored	Three additional coefficient sets can be stored in memory		

1.5 TAS5508A DAP Architecture

1.5.1 TAS5508A *DAP Architecture Diagrams*

Figure 1–4 shows the TAS5508A DAP architecture for Fs = 96 kHz. Note the TAS5508A bass management architecture shown in channels 1, 2, 7, and 8. Note that the I^2C registers are shown to help the designer configure the TAS5508A.

Figure 1–5 shows the TAS5508A architecture for Fs = 176.4 kHz or Fs = 192 kHz. Note that only channels 1, 2, and 8 contain all the features. Channels 3–7 are pass-through except for master volume control.

Figure 1–6 shows TAS5508A detailed channel processing. The output mixer is 8X2 for channels 1–6 and *X3 for channels 7 and 8.

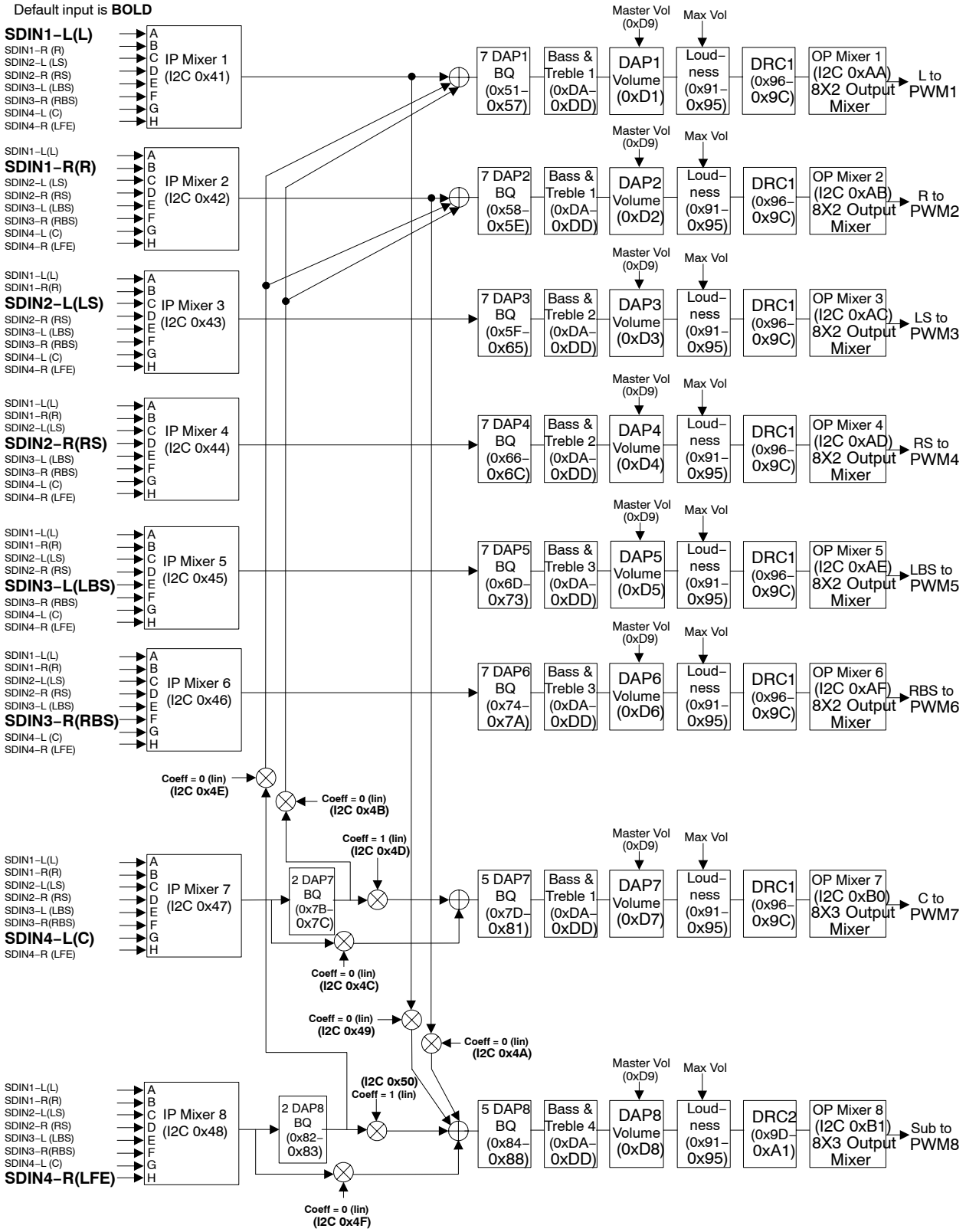


Figure 1–4. TAS5508A DAP Architecture With I²C Registers (Fs ≤ 96 kHz)

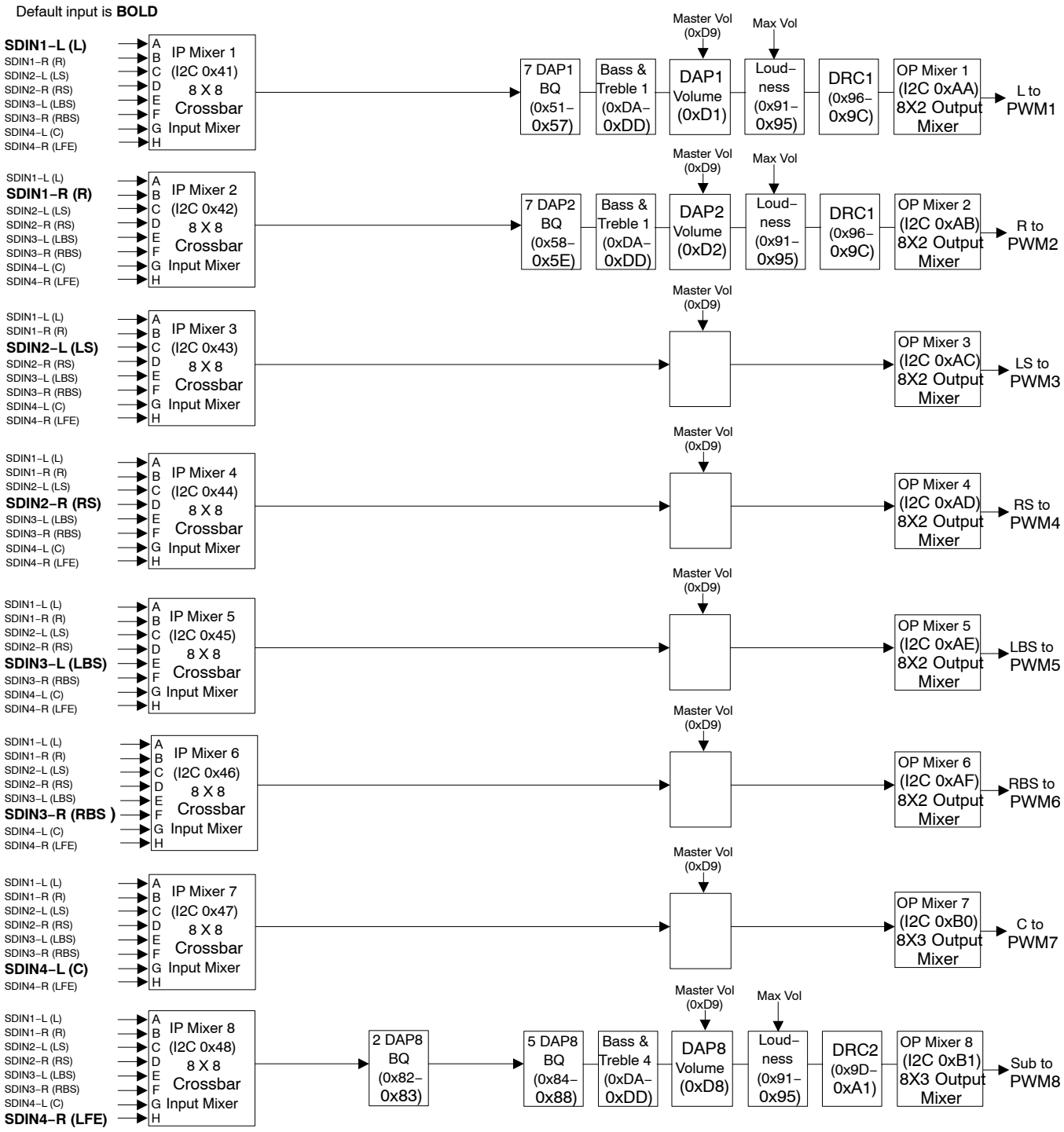


Figure 1–5. TAS5508A Architecture With I²C Registers (Fs = 176.4 kHz or Fs = 192 kHz)

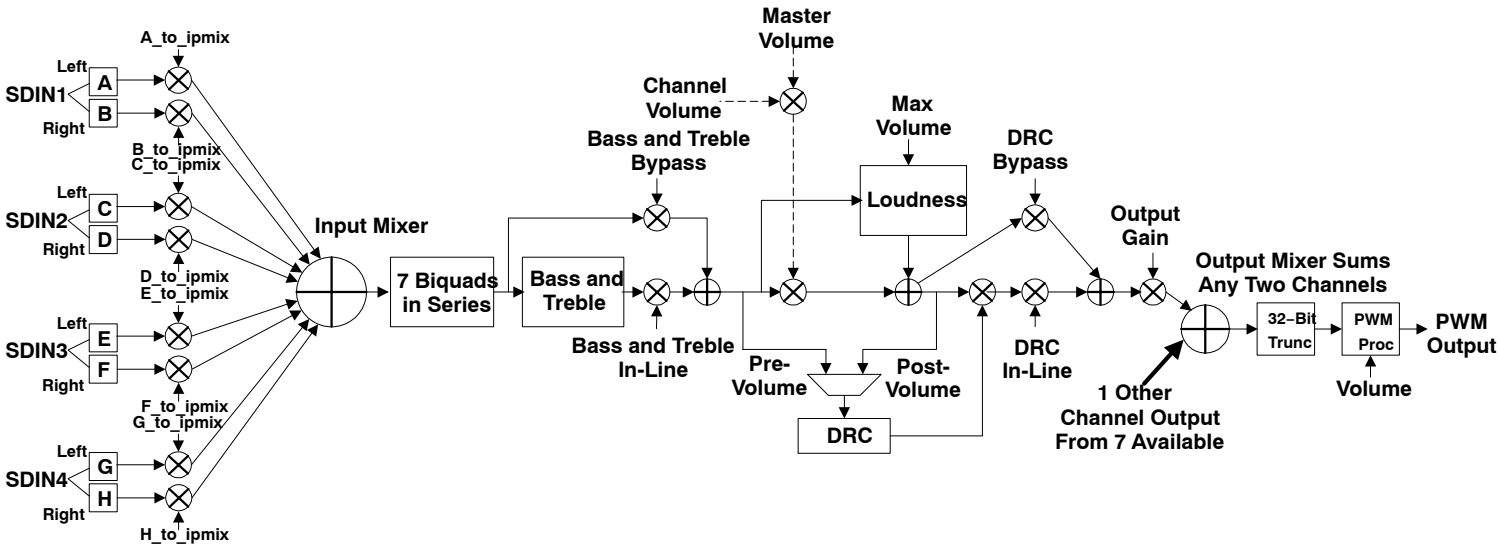


Figure 1–6. TAS5508A Detailed Channel Processing

1.5.2 I²C Coefficient Number Formats

The architecture of the TAS5508A is contained in ROM resources within the TAS5508A and cannot be altered. However, mixer gain, level offset, and filter tap coefficients, which can be entered via the I²C bus interface, provide a user with the flexibility to set the TAS5508A to a configuration that achieves the system level goals.

The firmware is executed in a 48-bit signed fixed-point arithmetic machine. The most significant bit of the 48-bit data path is a sign bit, and the 47 lower bits are data bits. Mixer gain operations are implemented by multiplying a 48-bit signed data value by a 28-bit signed gain coefficient. The 76-bit signed output product is then truncated to a signed 48-bit number. Level offset operations are implemented by adding a 48-bit signed offset coefficient to a 48-bit signed data value. In most cases, if the addition results in overflowing the 48-bit signed number format, saturation logic is used. This means that if the summation results in a positive number that is greater than 0x7FFF_FFFF_FFFF (the spaces are used to ease the reading of the hexadecimal number), the number is set to 0x7FFF_FFFF_FFFF. If the summation results in a negative number that is less than 0x8000_0000_0000 0000, the number is set to 0x8000_0000_0000 0000.

1.5.2.1 28-Bit 5.23 Number Format

All mixer gain coefficients are 28-bit coefficients using a 5.23 number format. Numbers formatted as 5.23 numbers means that there are 5 bits to the left of the decimal point and 23 bits to the right of the decimal point. This is shown in the Figure 1−7.

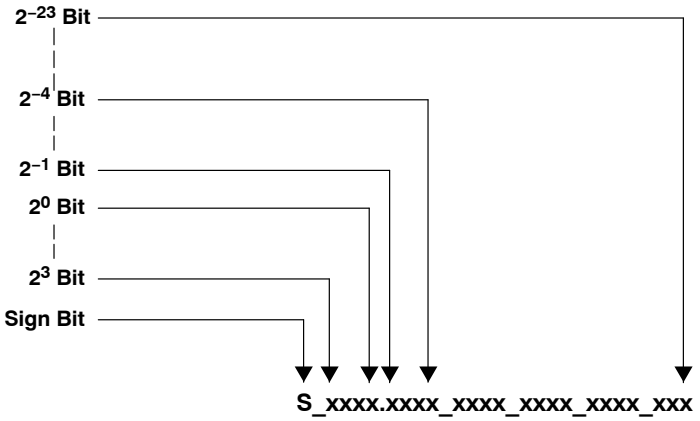


Figure 1−7. 5.23 Format

The decimal value of a 5.23 format number can be found by following the weighting shown in Figure 1−8. If the most significant bit is logic 0, the number is a positive number, and the weighting shown yields the correct number. If the most significant bit is a logic 1, then the number is a negative number. In this case every bit must be inverted, a 1 added to the result, and then the weighting shown in Figure 1−8 applied to obtain the magnitude of the negative number.

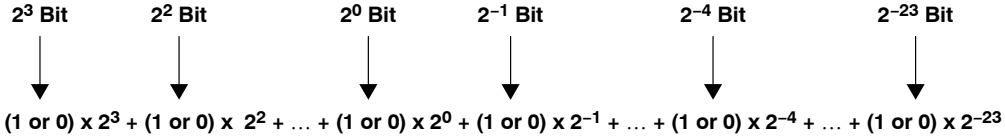
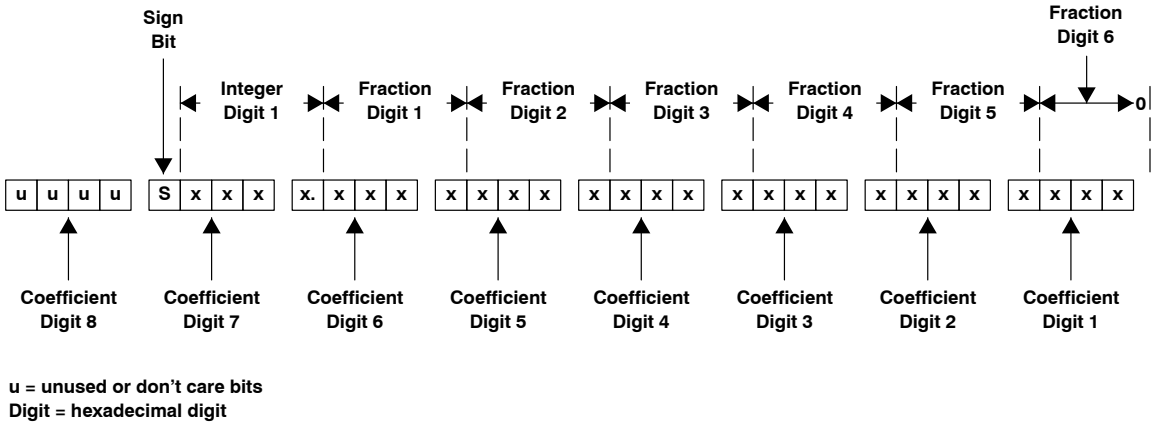


Figure 1−8. Conversion Weighting Factors—5.23 Format to Floating Point

Gain coefficients, entered via the I^2C bus, must be entered as 32-bit binary numbers. The format of the 32-bit number (4-byte or 8-digit hexadecimal number) is shown in Figure 1−9.



u = unused or don't care bits
Digit = hexadecimal digit

Figure 1−9. Alignment of 5.23 Coefficient in 32-Bit I^2C Word

As Figure 1−9 shows, the hex value of the integer part of the gain coefficient cannot be concatenated with the hex value of the fractional part of the gain coefficient to form the 32-bit I^2C coefficient. The reason is that the 28-bit coefficient contains 5 bits of integer, and thus the integer part of the coefficient occupies all of one hex digit and the most significant bit of the second hex digit. In the same way, the fractional part occupies the lower 3 bits of the second hex digit, and then occupies the other five hex digits (with the eighth digit being the zero-valued most significant hex digit).

1.5.2.2 48-Bit 25.23 Number Format

All level adjustment and threshold coefficients are 48-bit coefficients using a 25.23 number format. Numbers formatted as 25.23 numbers means that there are 25 bits to the left of the decimal point and 23 bits to the right of the decimal point. This is shown in Figure 1−10.

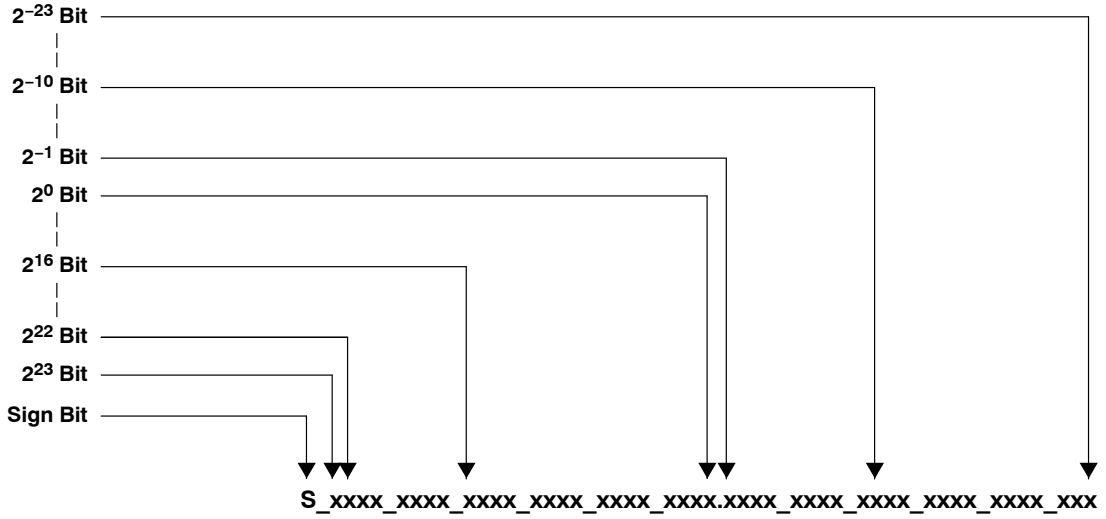


Figure 1−10. 25.23 Format

Figure 1−11 shows the derivation of the decimal value of a 48-bit 25.23 format number.

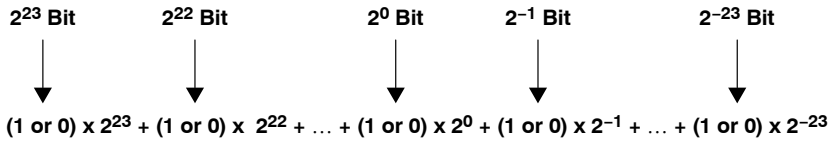


Figure 1−11. Alignment of 5.23 Coefficient in 32-Bit I²C Word

Two 32-bit words must be sent over the I²C bus to download a level or threshold coefficient into the TAS5508A. The alignment of the 48-bit, 25.23 formatted coefficient in the 8-byte (two 32-bit words) I²C word is shown in Figure 1−12.

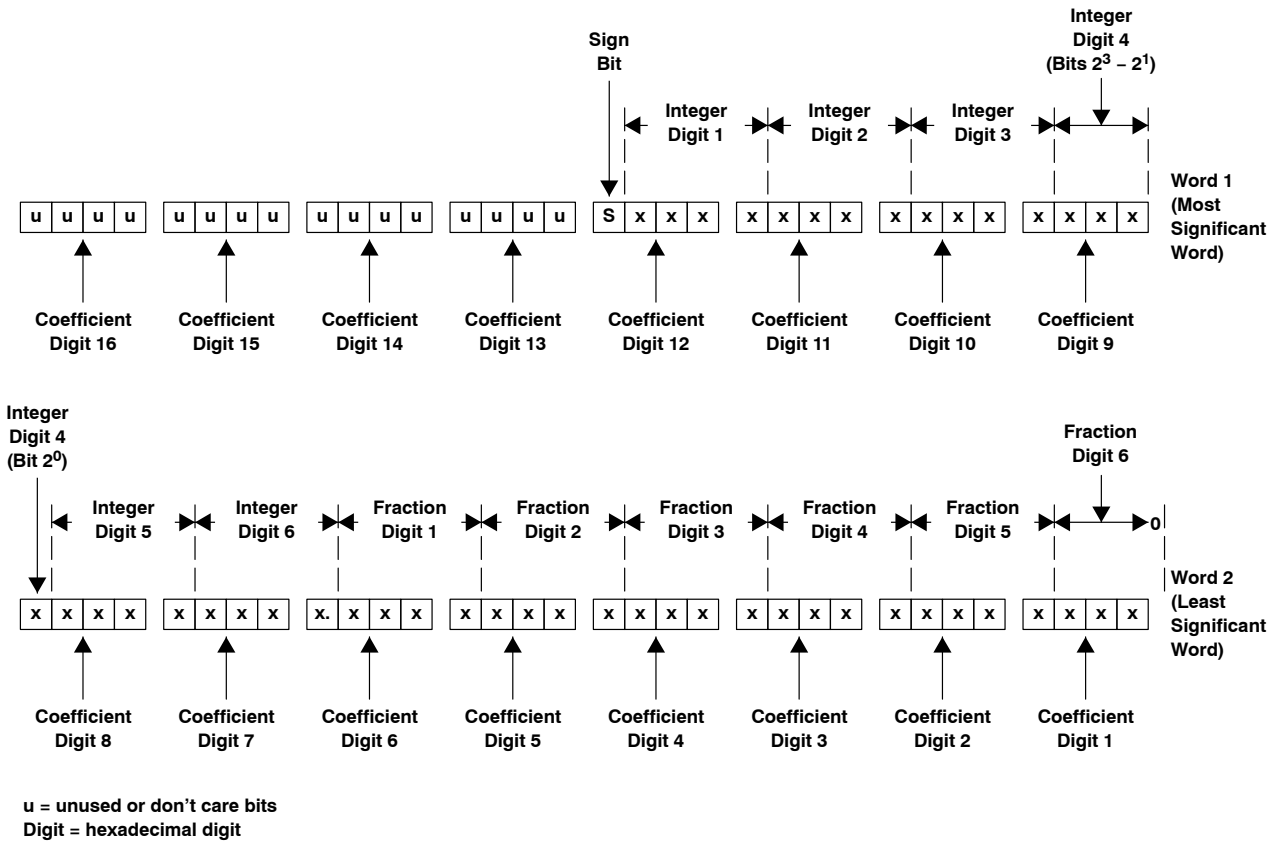


Figure 1–12. Alignment of 25.23 Coefficient in Two 32-Bit I²C Words

1.5.2.3 TAS5508A Audio Processing

The TAS5508A digital audio processing is designed such that noise produced by filter operations is maintained below the smallest signal amplitude of interest, as shown in Figure 1–13. The TAS5508A achieves this by increasing the precision of the signal representation substantially above the number of bits that are absolutely necessary to represent the input signal.

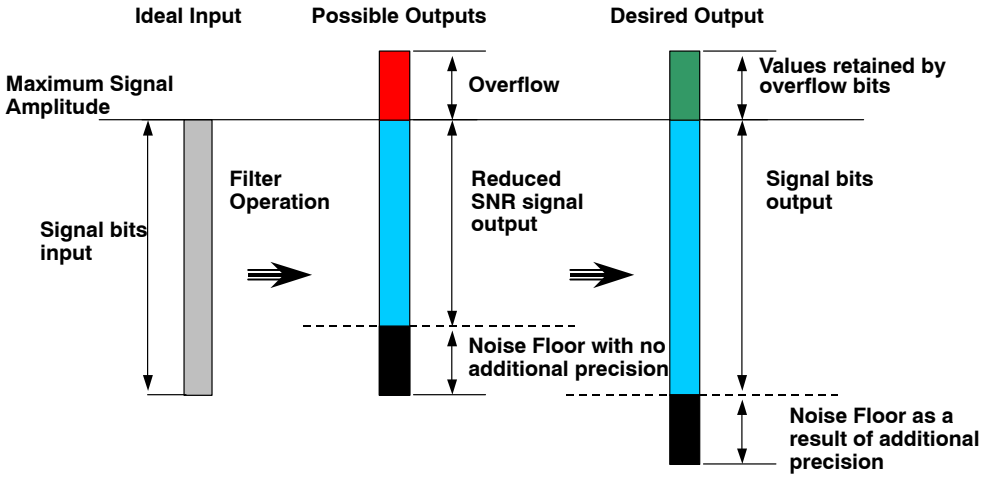


Figure 1–13. TAS5508A Digital Audio Processing

Similarly, the TAS5508A carries additional precision in the form of overflow bits to permit the value of intermediate calculations to exceed the input precision without clipping. The TAS5508A advanced digital audio processor achieves both of these important performance capabilities by using a high performance digital audio processing architecture with a 48-bit data path, 28-bit filter coefficients, and a 76-bit accumulator.

1.6 Input Crossbar Mixer

The TAS5508A has a full 8x8 input crossbar mixer. This mixer permits each signal processing channel input to be any ratio of any of the eight input channels. The control parameters for the input crossbar mixer are programmable via the I^{2}C interface. See the *Input Mixer Register (0x41–0x48, channels 1–8)* section.

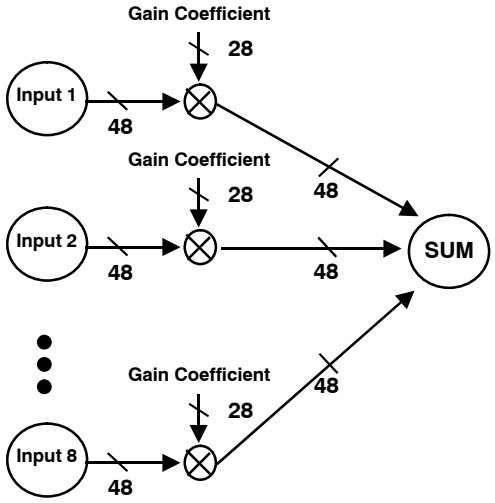


Figure 1–14. Input Crossbar Mixer

1.7 Biquad Filters

For 32-kHz to 96-kHz data, the TAS5508A provides 56 biquads across the eight channels (seven per channel)

For 176.4-kHz and 192-kHz data, the TAS5508A has 21 biquads across the three channels (seven per channel). All of the biquad filters are second order direct form I structure.

The direct form I structure provides a separate delay element and mixer (gain coefficient) for each node in the biquad filter. Each mixer output is a signed 76-bit product of a signed 48-bit data sample (25.23 format number) and a signed 28-bit coefficient (5.23 format number). The 76-bit ALU in the TAS5508A allows the 76-bit resolution to be retained when summing the mixer outputs (filter products).

The five 28-bit coefficients for the each of the 56 biquads are programmable via the I^{2}C interface. See Table 1−3.

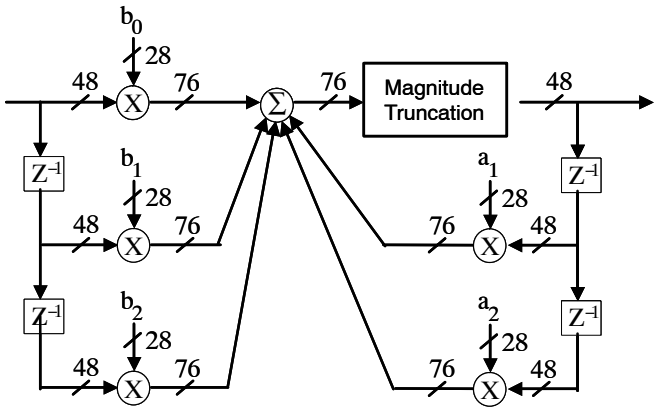


Figure 1−15. Biquad Filter Structure

All five coefficients for one biquad filter structure are written to one I^{2}C register containing 20 bytes (or five 32-bit words). The structure is the same for all biquads in the TAS5508A. Registers 0x51 − 0x88 show all the biquads in the TAS5508A. Note that u(31:28) bits are unused and default to 0x0.

Table 1−3. Contents of One 20-Byte Biquad Filter Register (Default = All-Pass)

DESCRIPTION	REGISTER FIELD CONTENTS	INITIALIZATION GAIN COEFFICIENT VALUE	
		DECIMAL	HEX
b_o Coefficient	u(31:28), b0(27:24), b0(23:16), b0(15:8), b0(7:0)	**1.0**	**0x00, 0x80, 0x00, 0x00**
b_1 Coefficient	u(31:28), b1(27:24), b1(23:16), b1(15:8), b1(7:0)	0.0	0x00, 0x00, 0x00, 0x00
b_2 Coefficient	u(31:28), b2(27:24), b2(23:16), b2(15:8), b2(7:0)	0.0	0x00, 0x00, 0x00, 0x00
a_1 Coefficient	u(31:28), a1(27:24), a1(23:16), a1(15:8), a1(7:0)	0.0	0x00, 0x00, 0x00, 0x00
a_2 Coefficient	u(31:28), a2(27:24), a2(23:16), a2(15:8), a2(7:0)	0.0	0x00, 0x00, 0x00, 0x00

1.8 Bass and Treble Controls

From 32-kHz to 96-kHz data, the TAS5508A has four Bass and Treble tone controls. Each control has a ±18-dB control range with selectable corner frequencies and 2nd order slopes. These controls operate four channel groups:

- L, R & C (Channels 1, 2, and 7)
- LS, RS (Channels 3 and 4)
- LBS, RBS (or alternately called L and R Lineout.) (Channels 5 and 6)
- Sub (Channel 8)

For 176.4 kHz and 192 kHz data, the TAS5508A has two Bass and Treble tone controls. Each control has a ±18-dB I^{2}C control range with selectable corner frequencies and 2nd order slopes. These controls operate two channel groups:

- L & R
- Sub

The bass and treble filters utilize a soft update rate that does not produce artifacts during adjustment.

Table 1–4. Bass and Treble Filter Selections

FS (kHz)	3-dB CORNER FREQUENCIES									
	FILTER SET 1	FILTER SET 1	FILTER SET 2	FILTER SET 2	FILTER SET 3	FILTER SET 3	FILTER SET 4	FILTER SET 4	FILTER SET 5	FILTER SET 5
	BASS	TREBLE	BASS	TREBLE	BASS	TREBLE	BASS	TREBLE	BASS	TREBLE
32	42	917	83	1833	125	3000	146	3667	167	4333
38	49	1088	99	2177	148	3562	173	4354	198	5146
44.1	57	1263	115	2527	172	4134	201	5053	230	5972
48	63	1375	125	2750	188	4500	219	5500	250	6500
88.2	115	2527	230	5053	345	8269	402	10106	459	11944
96	125	2750	250	5500	375	9000	438	11000	500	13000
176.4	230	5053	459	10106	689	16538	804	20213	919	23888
192	250	5500	500	11000	750	18000	875	22000	1000	26000

The I^2C registers that control Bass and Treble are:

- Bass and Treble By-Pass Register (0x89 – 0x90, channels 1–8)
- Bass and Treble Slew Rates (0xD0)
- Bass Filter Sets 1–5 (0xDA)
- Bass Filter Index (0xDB)
- Treble Filter Sets 1–5 (0xDC)
- Treble Filter Index (0xDD)

1.9 Volume, Automute, and Mute

The TAS5508A provides individual channel and master volume controls. Each control provides an adjustment range of +18.0618 dB to –100 dB in 0.25 dB increments. This permits a total volume device control range of +36 dB to –100 dB plus mute. The master volume control can be configured to control six or eight channels.

The TAS5508A has a master soft mute control that can be enabled by a terminal or I^2C command. The device also has individual channel soft mute controls that can are enabled via I^2C.

The soft volume and mute update rates are programmable. The soft adjustments are performed using a soft gain linear update with an I^2C programmable linear step size at a fixed temporal rate. The linear soft gain step size can be varied from 0.5 to 0.003906.

Table 1–5. Linear Gain Step Size

STEP SIZE (GAIN)	0.5	0.25	0.125	0.0625	0.03125	0.015625	0.007813	0.003906
Time to go from 36.124 db to –127 dB in ms	10.67	21.33	42.67	85.34	170.67	341.35	682.70	1365.4
Time to go from 18.062 db to –127 dB in ms	1.33	2.67	5.33	10.67	21.33	42.67	85.33	170.67
Time to go from 0 db to –127 dB in ms	0.17	0.33	0.67	1.33	2.67	5.33	10.67	21.33

1.9.1 Automute and Mute

The TAS5508A has individual channel automute controls that are enabled via the I²C interface. There are two separate detectors used to trigger the automute:

- Input automute: All channels are muted when all 8 inputs to the TAS5508A are less in magnitude than the input threshold value for a programmable amount of time.
- Output automute: A single channel is muted when the output of the DAP section is less in magnitude than the input threshold value for a programmable amount of time.

The detection period and thresholds for these two detectors are the same.

This time interval is selectable via I²C to be from 1 ms. to 110 ms. The increments of time are 1, 2, 3, 4, 5, 10, 20, 30, 40, 50, 60, 70, 80, 90, 100, and 110 ms. This interval is independent of the sample rate. The default value is mask programmable.

The input threshold value is an unsigned magnitude that is expressed as a bit position. This value is adjustable via I²C. The range of the input threshold adjustment is from below the LSB (bit position 0) to below bit position 12 in a 24 bit input data word (bit positions 8 to 20 in the DSPE). This provides an input threshold that can be adjusted for 12 to 24 bits of data. The default value is mask programmable.

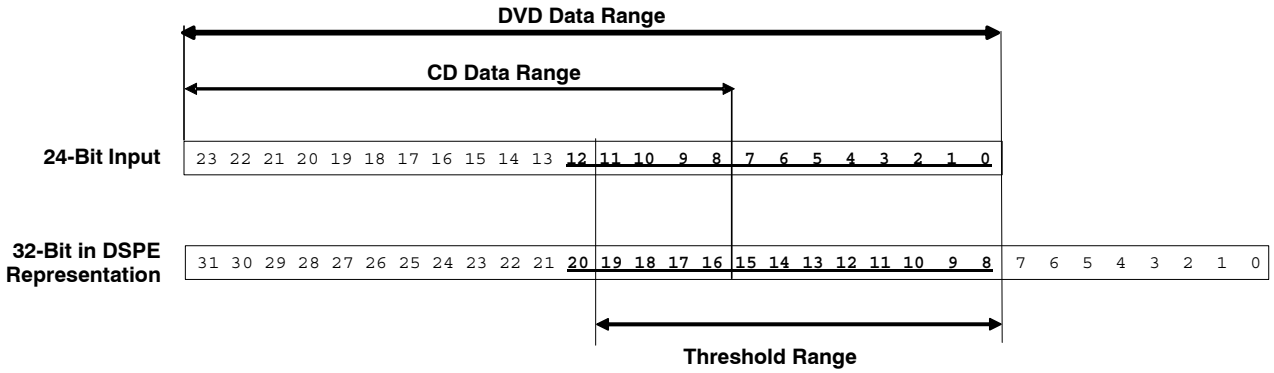


Figure 1–16. Automute Threshold

The automute state is exited when the TAS5508A receives one sample that is greater that the output threshold.

The output threshold can be one of two values:

- Equal to the input threshold
- 6 dB (one bit position) greater than the input threshold

The value for the output threshold is selectable via I²C. The default value is mask programmable.

The system latency enables the data value that is above the threshold to be preserved and output.

A mute command initiated by automute, master mute, individual I²C mute, the AM interference mute sequence, or the bank switch mute sequence overrides an unmute command or a volume command. While a mute command is activated, the commanded channels transition to the mute state. When a channel is unmuted, it goes to the last commanded volume setting that has been received for that channel.

1.10 Loudness Compensation

The loudness compensation function compensates for the Fletcher-Munson loudness curves. The TAS5508A loudness implementation tracks the volume control setting to provide spectral compensation for weak low or high frequency response at low volume levels. For the volume tracking function both linear and log control laws can be implemented. Any biquad filter response can be used to provide the desired loudness curve. The control parameters for the loudness control are programmable via the I²C interface.

The TAS5508A has a single set of loudness controls for the eight channels. In 6-channel mode loudness is available to the six speaker outputs and also the line outputs. The loudness control input uses the Maximum individual master volume (V) to control the loudness that is applied to all channels. In 192-kHz and 176.4-kHz modes, the loudness function is active only for channels 1, 2, and 8.

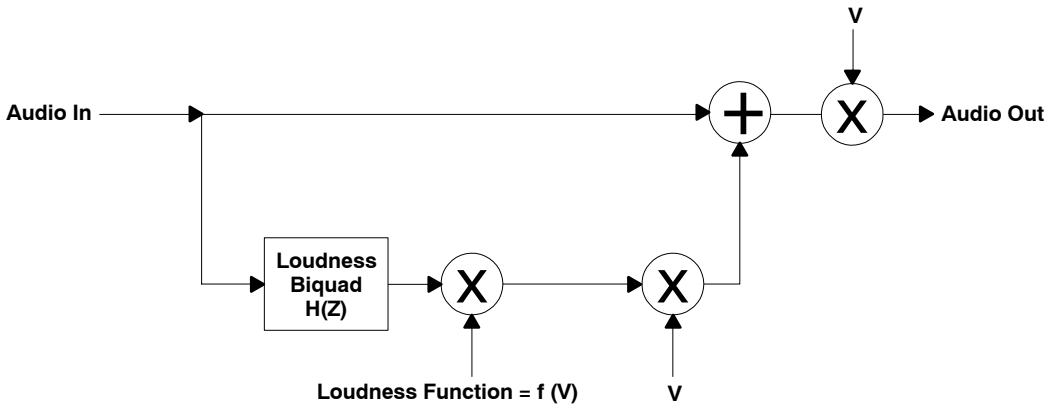


Figure 1–17. Loudness Compensation Functional Block Diagram

Loudness Function = f (V) = G x $[2^{[(\text{Log V}) \times \text{LG} + \text{LO}]}]$ + O or alternatively,

Loudness Function = f (V) = G x $[V^{\text{LG}} \times 2^{\text{LO}}]$ + O

For example, for the default values LG = –0.5, LO = 0.0, G = 1.0, and O = 0.0 then:

Loudness Function = 1 / SQRT (V) which is the recommended transfer function for loudness. So,

Audio Out = (Audio In) x V + H (Z) x SQRT (V). Other transfer functions are possible.

Table 1–6. Default Loudness Compensation Parameters

LOUDNESS TERM	DESCRIPTION	USAGE	DATA FORMAT	I^2C SUB-ADDRESS	DEFAULT	
					HEX	FLOAT
V	Max volume	Gains audio	5.23	NA	NA	NA
Log V	Log_2 (max volume)	Loudness function	5.23	NA	00000000	0.0
H (Z)	Loudness biquad	Controls shape of Loudness curves	5.23	0x95	b0 = 0000D513 b1 = 00000000 b2 = 0FFF2AED a1 = 00FE5045 a2 = 0F81AA27	b0 = 0.006503 b1 = 0 b2 = –0.006503 a1 = 1.986825 a2 = –0.986995
LG	Gain (log space)	Loudness function	5.23	0x91	FFC00000	–0.5
LO	Offset (log space)	Loudness function	25.23	0x92	00000000	0
G	Gain	Switch to enable Loudness (ON = 1, OFF = 0)	5.23	0x93	00000000	0
O	Offset	Provides offset	25.23	0x94	00000000	0

1.10.1 Loudness Example

Problem: Due to the Fletcher-Munson phenomena, we want to compensate for low frequency attenuation near 60 Hz. The TAS5508A provides a loudness transfer function with EQ gain = 6, EQ center frequency = 60 Hz, and EQ bandwidth = 60 Hz.

Solution: Using Texas Instruments ALE TAS5508A DSP tool, Matlab, or other signal-processing tool, develop a loudness function with following parameters:

Table 1–7. Loudness Function Parameters

LOUDNESS TERM	DESCRIPTION	USAGE	DATA FORMAT	I²C SUBADDRESS	EXAMPLE VALUES	
					HEX	FLOAT
H (Z)	Loudness Biquad	Controls shape of loudness curves	5.23	0x95	b0 = 00008ACE b1 = 00000000 b2 = FFFF7532 a1 = FF011951 a2 = 007EE914	b0 = 0.004236 b1 = 0 b2 = –0.004236 a1 = –1.991415 a2 = 0.991488
LG	Loudness Gain	Loudness function	5.23	0x91	FFC00000	–0.5
LO	Loudness Offset	Loudness function	25.23	0x92	00000000	0
G	Gain	Switch to Enable Loudness (ON = 1, OFF = 0)	5.23	0x93	00800000	1
O	Offset	Offset	25.23	0x94	00000000	0

See Figure 1–18 for the resulting loudness function at different gains.

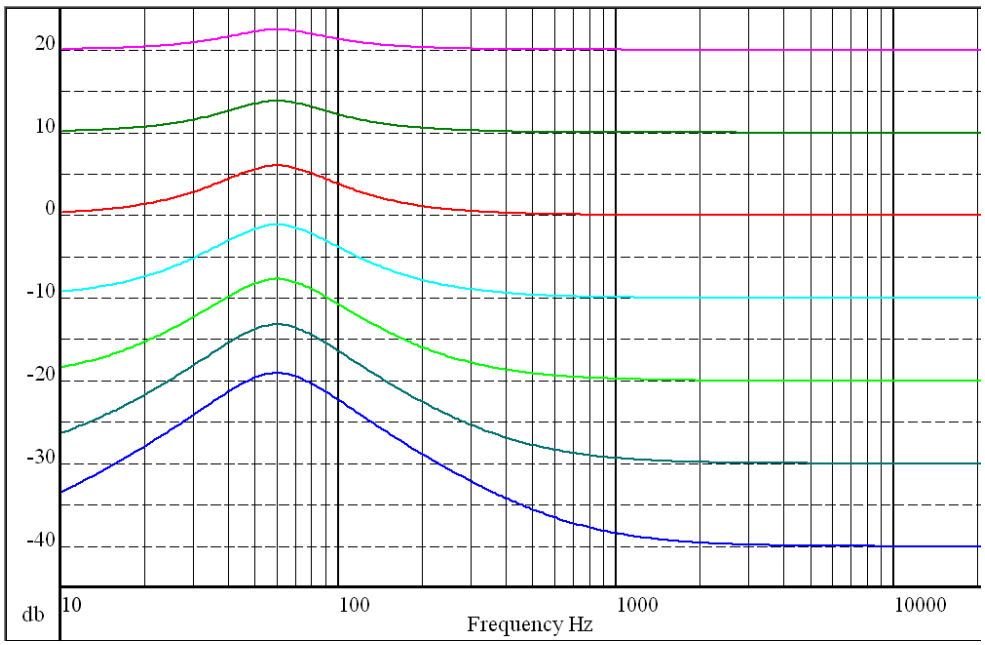


Figure 1–18. Loudness Example Plots

1.11 Dynamic Range Control (DRC)

The DRC provides both compression and expansion capabilities over three separate and definable regions of audio signal levels. Programmable threshold levels set the boundaries of the three regions. Within each of the three regions a distinct compression or expansion transfer function can be established and the slope of each transfer function is determined by programmable parameters. The offset (boost or cut) at the two boundaries defining the three regions can also be set by programmable offset coefficients. The DRC implements the composite transfer function by computing a 5.23 format gain coefficient from each sample output from the rms estimator. This gain coefficient is then applied to a mixer element, whose other input is the audio data stream. The mixer output is the DRC-adjusted audio data.

There are two distinct DRC blocks in the TAS5508A. DRC1 services channels 1–7 in the 8-channel mode and channels 1–4, and 7 in the 6-channel mode. This DRC computes rms estimates of the audio data streams on all channels that it controls. The estimates are then compared on a sample-by-sample basis and the larger of the estimates is used to compute the compression/expansion gain coefficient. The gain coefficient is then applied to appropriate channels audio stream. DRC2 services only channel 8. This DRC also computes an rms estimate of the signal level on channel 8 and this estimate is used to compute the compression/expansion gain coefficient applied to the channel 8 audio stream.

All of the TAS5508A default values for DRC can be used except for the DRC1 decay and DRC2 decay. Table 1–8 shows the recommended time constants and their HEX values. If the user wants to implement other DRC functions, Texas Instruments recommends using the automatic loudspeaker equalization (ALE) tool available from Texas Instruments. The ALE tool allows the user to select the DRC transfer function graphically. It will then output the TAS5508A hex coefficients for download to the TAS5508A.

Table 1–8. DRC Recommended Changes From TAS5508A Defaults

I²C SUBADDRESS	REGISTER FIELDS	RECOMMENDED TIME CONSTANT (MS)	RECOMMENDED HEX VALUE	DEFAULT HEX
0x98	DRC1 energy	5	0000883F	0000883F
	DRC1 (1 – energy)		007F77C0	007F77C0
0x9C	DRC1 attack	5	0000883F	0000883F
	DRC1 (1 – attack)		007F77C0	007F77C0
	DRC1 decay	2	0001538F	000000AE
	DRC1 (1 – decay)		007EAC70	007FFF51
0x9D	DRC2 energy	5	0000883F	0000883F
	DRC2 (1 – energy)		007F77C0	007F77C0
0xA1	DRC2 attack	5	0000883F	0000883F
	DRC2 (1 – attack)		007F77C0	007F77C0
	DRC2 decay	2	0001538F	000000AE
	DRC2 (1 – decay)		007EAC70	007FFF51

Recommended DRC set-up flow if the defaults are used:

- After power up, load the recommended hex value for DRC1 and DRC2 decay and (1 – decay). See Table 1–8.
- Enable either the pre-volume or post-volume DRC

Recommended DRC set-up flow if the DRC design uses values different from the defaults:

- After power up, load all DRC coefficients per the DRC design.
- Enable either the pre-volume or post-volume DRC

Figure 1–19 shows the positioning of the DRC block in the TAS5508A processing flow. As seen, the DRC input can come from either before or after soft volume control and loudness processing.

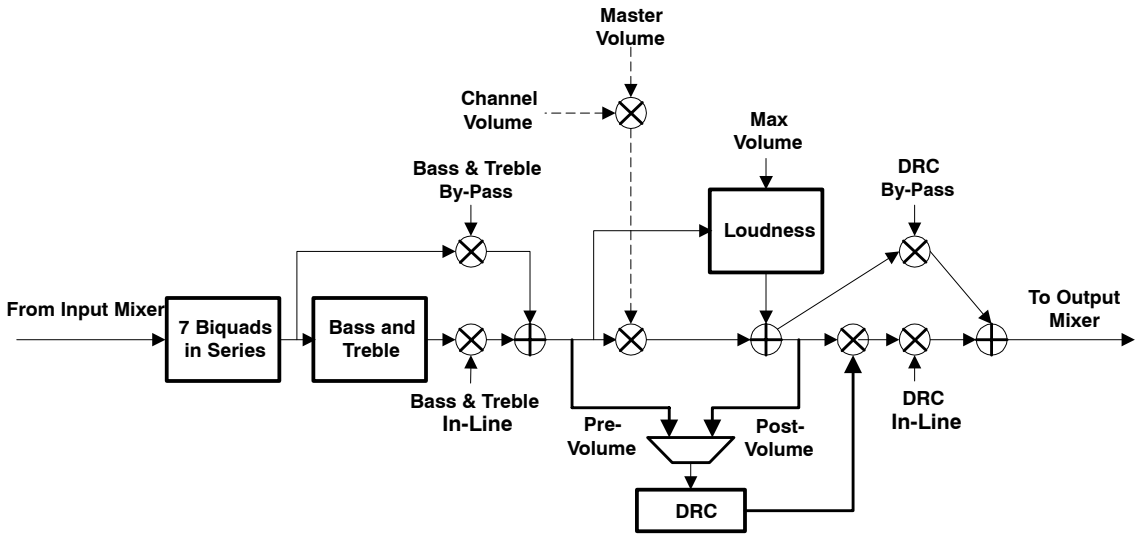


Figure 1–19. DRC Positioning in TAS5508A Processing Flow

Figure 1–20 illustrates a typical DRC transfer function.

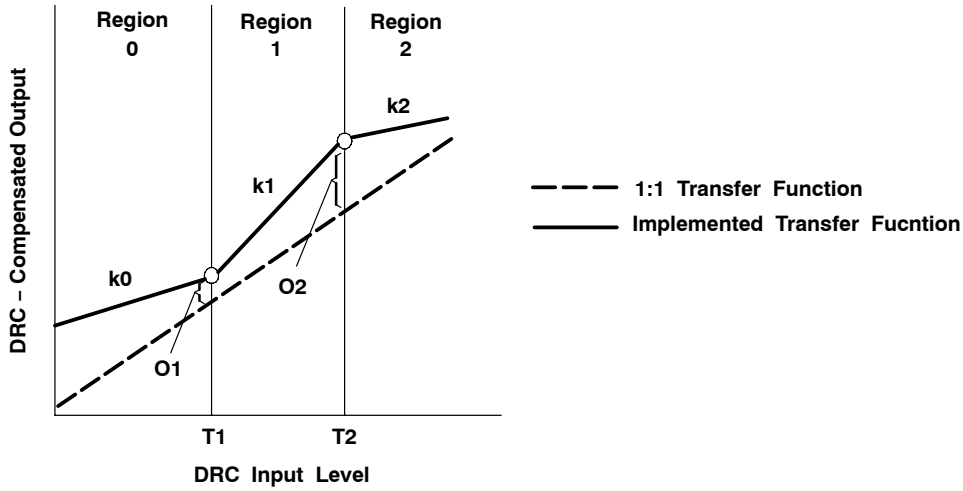


Figure 1–20. Dynamic Range Compression (DRC) Transfer Function Structure

The three regions shown in Figure 1–20 are defined by three sets of programmable coefficients:

- Thresholds T1 and T2—define region boundaries.
- Offsets O1 and O2—define the DRC gain coefficient settings at thresholds T1 and T2 respectively.
- Slopes k0, k1, and k2—define whether compression or expansion is to be performed within a given region. The magnitudes of the slopes define the degree of compression or expansion to be performed.

The three sets of parameters are all defined in logarithmic space and adhere to the following rules:

- The maximum input sample into the DRC is referenced at 0 dB. All values below this maximum value then have negative values in logarithmic (dB) space.
- The samples input into the DRC are 32-bit words and consist of the upper 32 bits of the 48-bit word format used by the digital audio processor (DAP). The 48-bit DAP word is derived from the 32-bit serial data received at the serial audio receive port by adding 8 bits of headroom above the 32-bit word and 8 bits of computational precision below the 32-bit word. If the audio processing steps between the SAP input and the DRC input result in no accumulative boost or cut, the DRC would operate on the 8 bits of headroom and the 24 MSBs of the audio sample. Under these conditions, a 0-dB (maximum value) audio sample (0x7FFFFFFF) is seen at the DRC input as a –48-dB sample (8 bits x –6.02 dB/bit = –48 dB).

- Thresholds T1 and T2 define, in dB, the boundaries of the three regions of the DRC, as referenced to the rms value of the data into the DRC. Zero valued threshold settings reference the maximum valued rms input into the DRC and negative valued thresholds reference all other rms input levels. Positive valued thresholds have no physical meaning and are not allowed. In addition, zero valued threshold settings are not allowed.

Although the DRC input is limited to 32-bit words, the DRC itself operates using the 48-bit word format of the DAP. The 32-bit samples input into the DRC are placed in the upper 32 bits of this 48-bit word space. This means that the threshold settings must be programmed as 48-bit (25.23 format) numbers.

CAUTION: Zero valued and positive valued threshold settings are not allowed and cause unpredictable behavior if used.

- Offsets O1 and O2 define, in dB, the attenuation (cut) or gain (boost) applied by the DRC-derived gain coefficient at the threshold points T1 and T2 respectively. Positive offsets are defined as cuts, and thus boost or gain selections are negative numbers. Offsets must be programmed as 48-bit (25.23 format) numbers.
- Slopes k0, k1, and k2 define whether compression or expansion is to be performed within a given region, and the degree of compression or expansion to be applied. Slopes are programmed as 28-bit (5.23 format) numbers.

1.11.1 DRC Implementation

The three elements comprising the DRC: (1) an rms estimator, (2) a compression/expansion coefficient computation engine, and (3) an attack/decay controller.

- RMS estimator—This DRC element derives an estimate of the rms value of the audio data stream into the DRC. For the DRC block shared by CH1 and CH2, two estimates are computed—an estimate of the CH1 audio data stream into the DRC, and an estimate of the CH2 audio data stream into the DRC. The outputs of the two estimators are then compared, sample-by-sample, and the larger valued sample is forwarded to the compression/expansion coefficient computation engine.

  Two programmable parameters, ae and (1 − ae), set the effective time window over which the rms estimate is made. For the DRC block shared by CH1 and CH2, the programmable parameters apply to both rms estimators. The time window over which the rms estimation is computed can be determined by:

$$t_{window} = \frac{-1}{F_S \, \ell n(1 - ae)}$$

- Compression/expansion coefficient computation—This DRC element converts the output of the rms estimator to a logarithmic number, determines the region that the input resides, and then computes and outputs the appropriate coefficient to the attack/decay element. Seven programmable parameters—T1, T2, O1, O2, k0, k1, and k2—define the three compression/expansion regions implemented by this element.
- Attack/decay control—This DRC element controls the transition time of changes in the coefficient computed in the compression/expansion coefficient computation element. Four programmable parameters define the operation of this element. Parameters ad and 1 − ad set the decay or release time constant to be used for volume boost (expansion). Parameters aa and 1 − aa set the attack time constant to be used for volume cuts. The transition time constants can be determined by:

$$t_a = \frac{-1}{F_S \, \ell n(1 - aa)} \qquad t_d = \frac{-1}{F_S \, \ell n(1 - ad)}$$

1.11.2 Compression/Expansion Coefficient Computation Engine Parameters

There are seven programmable parameters assigned to each DRC block: two threshold parameters - T1 and T2, two offset parameters - O1 and O2, and three slope parameters - k0, k1, and k2. The threshold parameters establish the three regions of the DRC transfer curve, the offsets anchor the transfer curve by establishing known gain settings at the threshold levels, and the slope parameters define whether a given region is a compression or an expansion region.

The audio input stream into the DRC must pass through DRC-dedicated programmable input mixers. These mixers are provided to scale the 32-bit input into the DRC to account for the positioning of the audio data in the 48-bit DAP word and the net gain or attenuation in signal level between the SAP input and the DRC. The selection of threshold values must take the gain (attenuation) of these mixers into account. The DRC implementation examples that follow illustrate the effect these mixers have on establishing the threshold settings.

T2 establishes the boundary between the high-volume region and the mid-volume region. T1 establishes the boundary between the mid-volume region and the low-volume region. Both thresholds are set in logarithmic space, and which region is active for any given rms estimator output sample is determined by the logarithmic value of the sample.

Threshold T2 serves as the fulcrum or pivot point in the DRC transfer function. O2 defines the boost (> 0 dB) or cut (< 0 dB) implemented by the DRC-derived gain coefficient for an rms input level of T2. If O2 = 0 dB, the value of the derived gain coefficient is 1.0 (0x00, 80, 00, 00 in 5.23 format). k2 is the slope of the DRC transfer function for rms input levels above T2 and k1 is the slope of the DRC transfer function for rms input levels below T2 (and above T1). The labeling of T2 as the fulcrum stems from the fact that there cannot be a discontinuity in the transfer function at T2. The user can, however, set the DRC parameters to realize a discontinuity in the transfer function at the boundary defined by T1. If no discontinuity is desired at T1, the value for the offset term O1 must obey the following equation.

$$O1_{\text{No Discontinuity}} = |T1 - T2| \times k1 + O2 \quad \text{For } (|T1| \geq |T2|)$$

T1 and T2 are the threshold settings in dB, k1 is the slope for region 1, and O2 is the offset in dB at T2. If the user chooses to select a value of O1 that does not obey the above equation, a discontinuity at T1 is realized.

Going down in volume from T2, the slope k1 remains in effect until the input level T1 is reached. If, at this input level, the offset of the transfer function curve from the 1:1 transfer curve does not equal O1, there is a discontinuity at this input level as the transfer function is snapped to the offset called for by O1. If no discontinuity is wanted, O1 and/or k1 must be adjusted so that the value of the transfer curve at the input level T1 is offset from the 1:1 transfer curve by the value O1. The examples that follow illustrate both continuous and discontinuous transfer curves at T1.

Going down in volume from T1, starting at the offset level O1, the slope k0 defines the compression/expansion activity in the lower region of the DRC transfer curve.

1.11.2.1 Threshold Parameter Computation

For thresholds,

$$T_{dB} = -6.0206T_{INPUT} = -6.0206T_{SUB_ADDRESS_ENTRY}$$

If, for example, it is desired to set T1 = -64 dB, then the subaddressaddress entry required to set T1 to -64 dB is:

$$T1_{SUB_ADDRESS_ENTRY} = \frac{-64}{-6.0206} = 10.63$$

T1 is entered as a 48-bit number in 25.23 format. Therefore:

T1 = 10.63 = 0_1010.1010_0001_0100_0111_1010_111
= 0x00000550A3D7 in 25.23 format

1.11.2.2 Offset Parameter Computation

The offsets set the boost or cut applied by the DRC-derived gain coefficient at the threshold point. An equivalent statement is that offsets represent the departure of the actual transfer function from a 1:1 transfer at the threshold point. Offsets are 25.23 formatted 48-bit logarithmic numbers. They are computed by the following equation.

$$O_{INPUT} = \frac{O_{DESIRED} + 24.0824\ dB}{6.0206}$$

Gains or boosts are represented as negative numbers; cuts or attenuation are represented as positive numbers. For example, to achieve a boost of 21 dB at threshold T1, the I^2C coefficient value entered for O1 must be:

$$O1_{INPUT} = \frac{-21\ dB + 24.0824\ dB}{6.0206} = 0.51197555$$
$$= 0.1000_0011_0001_1101_0100$$
$$= 0x00000041886A \text{ in } 25.23 \text{ format}$$

More examples of offset computations are included in the following examples.

1.11.2.3 Slope Parameter Computation

In developing the equations used to determine the subaddress of the input value required to realize a given compression or expansion within a given region of the DRC, the following convention is adopted.

DRC Transfer = Input Increase : Output Increase

If the DRC realizes an output increase of n dB for every dB increase in the rms value of the audio into the DRC, a 1:n expansion is being performed. If the DRC realizes a 1 dB increase in output level for every n dB increase in the rms value of the audio into the DRC, a n:1 compression is being performed.

For 1:n expansion, the slope k can be found by:

$k = n - 1$

For n:1 compression, the slope k can be found by: $k = \frac{1}{n} - 1$

In both expansion (1:n) and compression (n:1), n is implied to be greater than 1. Thus, for expansion:

$k = n - 1$ means $k > 0$ for $n > 1$. Likewise, for compression, $k = \frac{1}{n} - 1$ means $-1 < k < 0$ for $n > 1$. Thus, it appears that k must always lie in the range $k > -1$.

The DRC imposes no such restriction and k can be programmed to values as negative as −15.999. To determine what results when such values of k are entered, it is first helpful to note that the compression and expansion equations for k are actually the same equation. For example, a 1:2 expansion is also a 0.5:1 compression.

$$0.5 \text{ Compression} \Rightarrow k = \frac{1}{0.5} - 1 = 1$$

$$1:2 \text{ Expansion} \Rightarrow k = 2 - 1 = 1$$

As can be seen, the same value for k is obtained either way. The ability to choose values of k less than −1 allows the DRC to implement negative slope transfer curves within a given region. Negative slope transfer curves are usually not associated with compression and expansion operations, but the definition of these operations can be expanded to include negative slope transfer functions. For example, if $k = -4$

$$\text{Compression Equation : } k = -4 = \frac{1}{n} - 1 \Rightarrow n = -\frac{1}{3} \Rightarrow -0.3333 : 1 \text{ compression}$$

$$\text{Expansion Equation : } k = -4 = n - 1 \Rightarrow n = -3 \Rightarrow 1 : -3 \text{ expansion}$$

With $k = -4$, the output decreases 3 dB for every 1 dB increase in the rms value of the audio into the DRC. As the input increases in volume, the output decreases in volume.

1.12 Output Mixer

The TAS5508A provides an 8x2 output mixer for channels 1, 2, 3, 4, 5, and 6. For channels 7 and 8 the TAS5508A provides an 8x3 output mixer. These mixers allow each output to be any ratio of any two (three) signal processed channels. The control parameters for the output crossbar mixer are programmable via the I^2C interface.

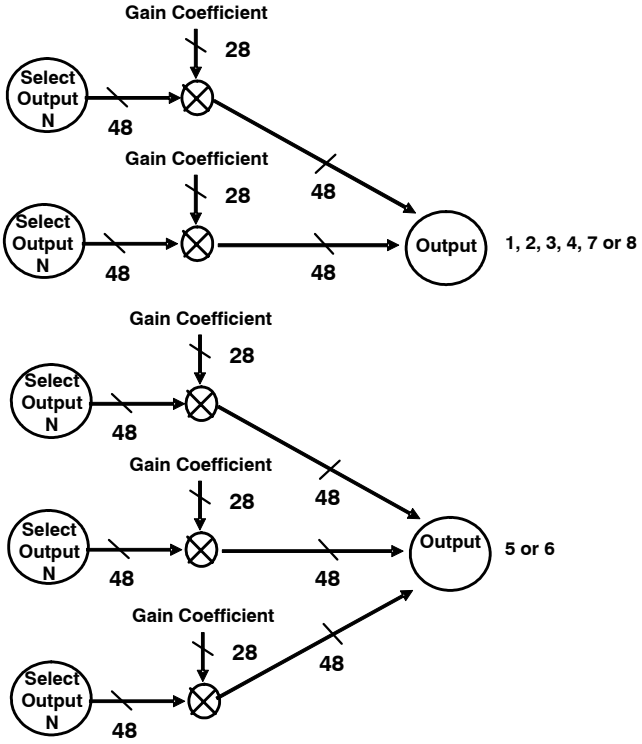


Figure 1–21. Output Mixers

1.13 PWM

The TAS5508A has eight channels of high performance digital PWM Modulators that are designed to drive switching output stages (backends) in both single-ended (SE) and H-bridge (bridge tied load) configuration. The TAS5508A device uses noise-shaping and sophisticated error correction algorithms to achieve high power efficiency and high-performance digital audio reproduction. The TAS5508A uses an AD1 PWM modulation combined with a 5^{th} order noise shaper to provide a 102-dB SNR from 20 to 20 kHz.

The PWM section accepts 32-bit PCM data from the DAP and outputs eight PWM audio output channels configurable as either:

- Six channels to drive power stages + two channels to drive a differential input active filter to provide a separately controllable stereo line out
- Eight channels to drive power stages

The TAS5508A PWM section output supports both single-ended and bridge-tied loads.

The PWM section provides a headphone PWM output to drive an external differential amplifier like the TPA112. The headphone circuit uses the PWM modulator for channels 1 and 2. The headphone will not operate while the six or eight backend drive channels are operating. The headphone will be enabled via a headphone select terminal or I^2C command.

The PWM section has individual channel dc blocking filters that can be enabled and disabled. The filter cutoff frequency is less than 1 Hz.

The PWM section has individual channel de-emphasis filters for 32, 44.1, and 48 kHz that can be enabled and disabled.

The PWM section also contains the power supply volume control (PSVC) PWM.

The interpolator, noise shaper, and PWM sections provide a PWM output with the following features:

- Up to 8x over sampling.
  - 8x at F_S = 44.1 kHz, 48 kHz, 32 kHz, 38 kHz
  - 4x at F_S = 88.2 kHz, 96 kHz
  - 2x at F_S = 176.4 kHz, 192 kHz
- 5th order noise shaping
- 100-dB dynamic range 0 – 20 kHz (TAS5508A + TAS5111 system measured at speaker terminals)
- THD < 0.01%
- Adjustable maximum modulation limit of 93.8% to 99.2%
- 3.3-V digital signal

1.13.1 DC Blocking (High Pass Enable/ Disable)

Each input channel incorporates a first order digital high-pass filter to block potential dc components. The filter –3 dB point is approximately 0.89-Hz at 44.1-kHz sampling rate. The high-pass filter can be enabled and disabled via the I^2C interface.

1.13.2 De-Emphasis Filter

For audio sources that have been pre-emphasized, a precision 50 μs/15 μs de-emphasis filter is provided to support the sampling rates of 32 kHz, 44.1 kHz, and 48 kHz. Figure 1–22 shows a graph of the de-emphasis filtering characteristics. De-emphasis is set using two bits in the system control register.

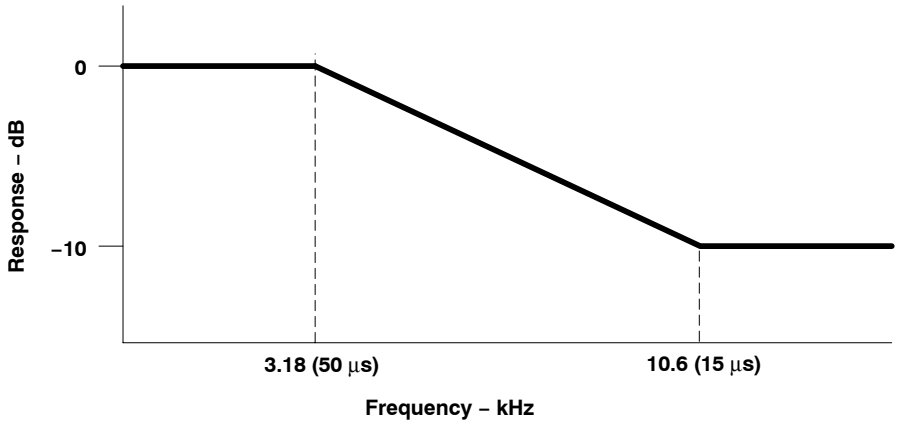


Figure 1–22. De-emphasis Filter Characteristics

1.13.3 Power Supply Volume Control (PSVC)

The TAS5508A supports volume control by both conventional digital gain / attenuation and by a combination of digital and analog gain / attenuation. Varying the H-bridge power supply voltage performs the analog volume control function. The benefits of using powers supply volume control (PSVC) are reduced idle channel noise, improved signal resolution at low volumes, increased dynamic range, and reduced radio frequency emissions at reduced power levels. The power supply volume control (PSVC) is enabled via I^2C. When enabled the PSCV provides a PWM output that is filtered to provide a reference voltage for the power supply. The power supply adjustment range can be set for –12.04, –18.06, or –24.08 dB, to accommodate a range of variable power supply designs.

Figure 1–23 and Figure 1–24 show how power supply and digital gains can be used together.

The volume biquad (0xCF) can be used to implement a low-pass filter in the digital volume control to match the PSVC volume transfer function.

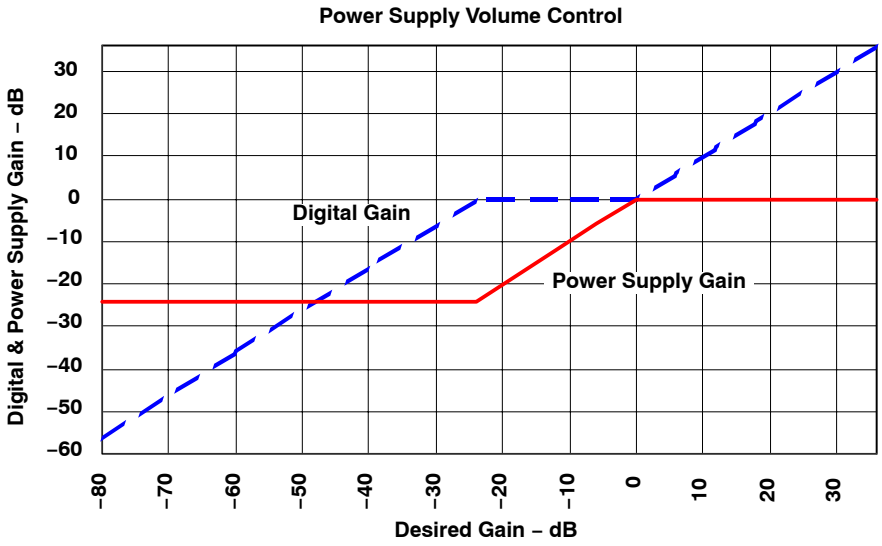


Figure 1–23. Power Supply and Digital Gains (Log Space)

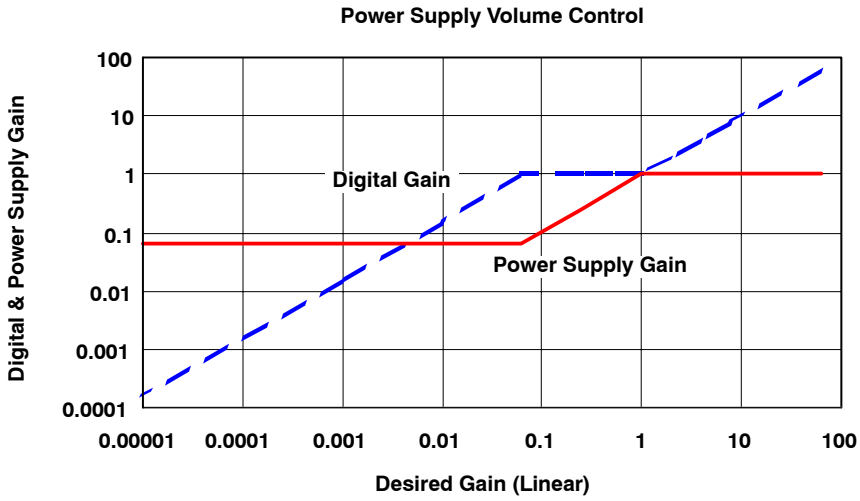


Figure 1–24. Power Supply and Digital Gains (Linear Space)

1.13.4 AM Interference Avoidance

Digital amplifiers can degrade AM reception as a result of their RF emissions. Texas Instruments patented AM interference avoidance circuit provides a flexible system solution for a wide variety of digital audio architectures. During AM reception, the TAS5508A adjusts the radiated emissions to provide an emission clear zone for the tuned AM frequency. The inputs to the TAS5508A for this operation are the tuned AM frequency, the IF frequency, and the sample rate. The sample rate is automatically detected.

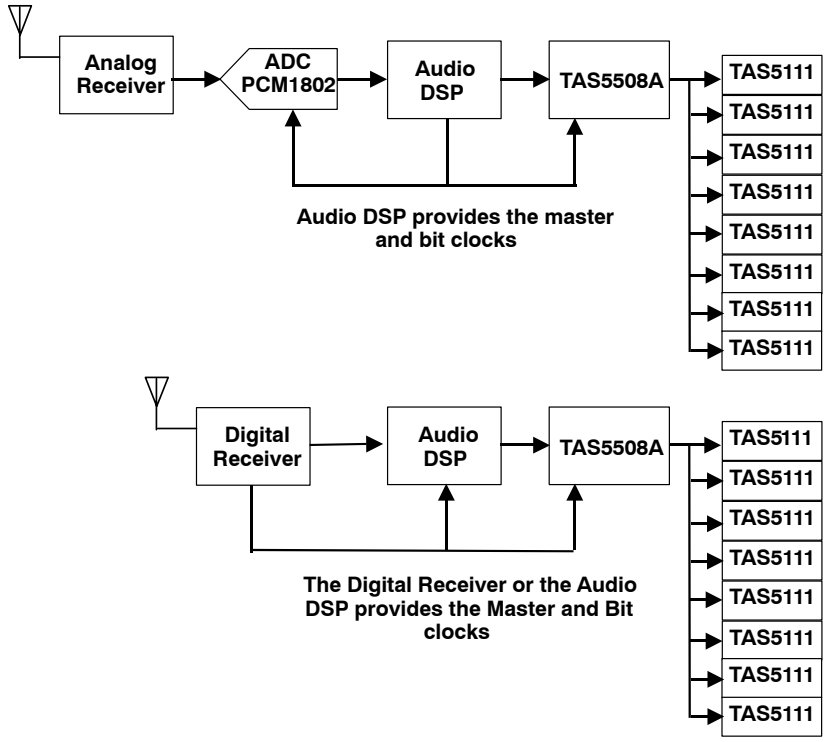


Figure 1–25. Block Diagrams of Typical Systems Requiring TAS5508A Automatic AM Interference Avoidance Circuit

2 TAS5508A Controls and Status

The TAS5508A provides control and status information from both the I²C registers and device pins.

This section describes some of these controls and status functions. The I²C summary and detailed register descriptions are contained in sections at the end of this document.

2.1 I²C Status Registers

The TAS5508A has two status registers that provide general device information. These are the General Status Register 0 (0x01) and the Error Status Register (0x02).

2.1.1 General Status Register (0x01)

- Device identification code
- Clip indicator – The TAS5508A has a clipping indicator. Writing to the register clears the indicator.
- Bank switching is busy

2.1.2 Error Status Register (0x02)

- No internal errors (the valid signal is high)
- A clock error has occurred – These are sticky bits that are cleared by writing to the register.
  - LRCLK error – When the number of MCLKs per LRCLK is incorrect
  - SCLK error – When the number of SCLKS per LRCLK is incorrect
  - Frame slip – When the number of MCLKs per LRCLK changes by more than 10 MCLK cycles
  - PLL phase-lock error
- This error status register is normally used for system development only.

2.2 TAS5508A Pin Controls

The TAS5508A provide a number of terminal controls to manage the device operation. These controls are:

- $\overline{\text{RESET}}$
- $\overline{\text{PDN}}$
- $\overline{\text{BKND_ERR}}$
- $\overline{\text{HP_SEL}}$
- $\overline{\text{MUTE}}$

2.2.1 Reset ($\overline{\text{RESET}}$)

The TAS5508A is placed in the reset mode by setting the $\overline{\text{RESET}}$ terminal low or by the power up reset circuitry when power is applied.

$\overline{\text{RESET}}$ is an asynchronous control signal that restores the TAS5508A to the hard mute state (M). Master volume is immediately set to full attenuation (there is no ramp down). Reset initiates the device reset without an MCLK input. As long as the $\overline{\text{RESET}}$ terminal is held low, the device is in the reset state. During reset, all I²C and serial data bus operations are ignored.

Table 2–1 shows the device output signals while $\overline{\text{RESET}}$ is active.

Table 2–1. Device Outputs During Reset

SIGNAL	SIGNAL STATE
Valid	Low
PWM P-outputs	Low (M-State)
PWM M-outputs	Low (M-State)
SDA	Signal Input (not driven)

Because $\overline{\text{RESET}}$ is an asynchronous signal, clicks and pops produced during the application (the leading edge) of $\overline{\text{RESET}}$ cannot be avoided. However, the transition from the hard mute state (M) to the operational state is performed using a quiet start up sequence to minimize noise. This control uses the PWM reset and unmute sequence to shut down and start up the PWM. A detailed description of these sequences is contained in the PWM section. If a completely quiet reset or power down sequence is desired, $\overline{\text{MUTE}}$ should be applied before applying $\overline{\text{RESET}}$.

The rising edge of the reset pulse begins device initialization before the transition to the operational mode. During device initialization, all controls are reset to their initial states. Table 2–2 shows the default control settings following a reset.

Table 2–2. Values Set During Reset

CONTROL	SETTING
Clock register	Not valid
High pass	Disabled
Unmute from clock error	Hard unmute
PSVC high Z	Disabled
Post DAP detection automute	Enabled
Eight Ch PreDAP detection automute	Enabled
De–emphasis	De-emphasis disabled
Channel configuration control	Configured for the default setting
Headphone configuration control	Configured for the default setting
Serial data interface format	I^2S 24 bit
Individual channel mute	No channels are muted
Automute delay	5 ms
Automute threshold 1	< 8 bits
Automute threshold 2	Same as automute threshold 1
Modulation limit	Maximum modulation limit of 97.7%
Six (or eight – low) channel configuration	Eight channels
Slew rate limit	Disengaged for all channels
Interchannel delay	–32, 0, –16, 16, –24, 8, –8, –24
Shutdown PWM on error	Enabled
Volume and mute update rate	Volume ramp 85 ms
Treble and bass slew rate	Update every 1.31 ms
Bank switching	Manual bank selection is enabled
Auto bank switching map	All channels use Bank 1
Biquad coefficients (5508)	Set to All pass
Input mixer coefficients	Input N –> Channel N, no attenuation
Output mixer coefficients	Channel N –> Output N, no attenuation
Subwoofer sum into Ch1 and 2 (5508)	Gain of 0
Ch1 and 2 sum in subwoofer (5508)	Gain of 0
Bass and treble bypass	Gain of 1
Bass and treble Inline	Gain of 0
DRC bypass (5508)	Gain of 1
DRC inline (5508)	Gain of 0
DRC (5508)	DRC disabled, default values
Master volume	Mute
Individual channel volumes	0 dB
All bass and treble Indexes	0x12 neutral
Treble filter sets	Filter Set 3

CONTROL	SETTING
Bass filter sets	Filter Set 3
Loudness (5508)	Loudness disabled, default values
AM interference enable	Disabled
AM interference IF	455
AM interference select sequence	1
Tuned freq and mode	0000 , BCD
Subwoofer PSVC control	Enabled
PSVC and PSVC range	Disabled / 0 dB

After the initialization time, the TAS5508A starts the transition to the operational state with the Master volume set at mute.

Since the TAS5508A has an external crystal time base, following the release of RESET, the TAS5508A sets the MCLK and data rates and perform the initialization sequences. The PWM outputs are held at a mute state until the master volume is set to a value other than mute via I^2C.

2.2.2 Power Down ($\overline{PDN}$)

TheTAS5508A can be placed into the power down mode by holding the $\overline{PDN}$ terminal low. When power down mode is entered, both the PLL and the oscillator are shut down. Volume is immediately set to full attenuation (there is no ramp down). This control uses the PWM mute sequence that provides a low click and pop transition to the hard mute state (M). A detailed description of the PWM mute sequence is contained in the PWM section.

Power down is an asynchronous operation that does not require MCLK to go into the power down state. To initiate the power-up sequence requires MCLK to be operational and the TAS5508A to receive 5 MCLKs prior to the release of $\overline{PDN}$.

As long as the $\overline{PDN}$ terminal is held low the device is in the power down state with the PWM outputs in a hard mute (M) state. During power down, all I^2C and serial data bus operations are ignored. Table 2–3 shows the device output signals while $\overline{PDN}$ is active.

Table 2–3. Device Outputs During Power Down

SIGNAL	SIGNAL STATE
Valid	Low
PWM P-outputs	M-state = low
PWM M-outputs	M-state = low
SDA	Signal input
PSVC	M-state = low

Following the application of $\overline{PDN}$, the TAS5508A does not perform a quiet shutdown to prevent clicks and pops produced during the application (the leading edge) of this command. The application of $\overline{PDN}$ immediately performs a PWM stop. A quiet stop sequence can be performed by first applying $\overline{MUTE}$ before $\overline{PDN}$.

When $\overline{PDN}$ is released, the system goes to the end state specified by $\overline{MUTE}$ and $\overline{BKND_ERR}$ pins and the I^2C register settings.

The crystal time base allows the TAS5508A to determine the CLK rates. Once these rates are determined, the TAS5508A unmutes the audio.

2.2.3 Backend Error ($\overline{BKND_ERR}$)

Backend error is used to provide error management for backend error conditions. Backend error is a level sensitive signal. Backend error can be initiated by bringing the $\overline{BKND_ERR}$ terminal low for a minimum 5 MCLK cycles. When $\overline{BKND_ERR}$ is brought low, the PWM sets either six or eight channels into the PWM backend error state. This state is described in the PWM section. Once the backend error sequence is initiated, a delay of 5 ms is performed before the system starts the output re–initialization sequence. After the initialization time, the TAS5508A begins normal operation. Backend error does not affect other PWM modulator operations

The number of channels that are affected by the $\overline{\text{BKND_ERR}}$ signal is dependent upon the 6-channel configuration signal. If the I^2C setting 6-channel configuration is false, the TAS5508A places all eight PWM outputs in the PWM backend error state, while not affecting any other internal settings or operations. If the I^2C setting six configuration is true, the TAS5508A brings the PWM outputs 1−6 to a backend error state, while not affecting any other internal settings or operations. Table 2−4 shows the device output signal states during backend error.

Table 2−4. Device Outputs During Backend Error

SIGNAL	SIGNAL STATE
Valid	Low
PWM P-outputs	M-State – low
PWM M-outputs	M-State – low
HPPWM P-outputs	M-State – low
HPPWM M-outputs	M-State – low
SDA	Signal Input (not driven)

2.2.4 Speaker / Headphone Selector ($\overline{\text{HP_SEL}}$)

The $\overline{\text{HP_SEL}}$ terminal enables the headphone output or the speaker outputs. The headphone output receives the processed data output from DAP and PWM channels 1 and 2.

In 6-channel configuration this feature does not affect the two lineout channels.

When low, the headphone output is enabled. In this mode the speaker outputs are disabled. When high, the speaker outputs are enabled and the headphone is disabled.

Changes in the pin logic level results in a state change sequence using soft mute to the hard mute (M) state for both speaker and headphone followed by a soft unmute.

When $\overline{\text{HP_SEL}}$ is low, the configuration of channels 1 and 2 are defined by the headphone configuration register. When HP_SEL is high, the channel 1 and 2 configuration registers define the configuration of channels 1 and 2.

2.2.5 Mute ($\overline{\text{MUTE}}$)

The mute control provides a noiseless volume ramp to silence. Releasing mute provides a noiseless ramp to previous volume. The TAS55508 has both a master and individual channel mute commands. A terminal is also provided for the master MUTE. The low active master Mute I^2C register and the $\overline{\text{MUTE}}$ terminal are logically Or'ed together. If either is set to low, a mute on all channels is performed. The master mute command operates on all channels regardless on whether the system is in six or eight channel configuration.

When MUTE is invoked, the PWM output stops switching and then goes to an idle state.

The master Mute terminal is used to support a variety of other operations in the TAS5508A, such as setting the inter-channel delay, the biquad coefficients, the serial interface format, and the clock rates. A mute command by the master mute terminal, individual I^2C mute, the AM interference mute sequence, the bank switch mute sequence, or automute overrides an unmute command or a volume command. While a mute is active, the commanded channels will be placed in a mute state. When a channel is unmuted, it goes to the last commanded volume setting that has been received for that channel.

2.3 Device Configuration Controls

The TAS5508A provides a number of system configuration controls that are set at initialization and following a reset.

- Channel Configuration
- Headphone Configuration
- Audio System Configurations

- Recovery from Clock Error
- Power Supply Volume Control Enable
- Volume and Mute Update Rate
- Modulation Index Limit
- Inter-channel Delay
- Master Clock and Data Rate Controls
- Bank Controls

2.3.1 Channel Configuration Registers

In order for the TAS5508A to have full control of the power stages, registers 0x05 to 0x0C must be programmed to reflect the proper power stage and how each one should be controlled. Channel configuration registers consist of eight registers, one for each channel.

The primary reason for using these registers is that different power stages require different handling during start up, mute/unmute, shutdown, and error recovery. The TAS5508A must select the sequence that gives the best click and pop performance and insure that the bootstrap capacitor is charged correctly during start up. This sequence depends on which power stage is present at the TAS5508A output.

Table 2–5. Description of the Channel Configuration Registers (0x05 to 0x0C)

BIT	DESCRIPTION
D7	Enable/disable error recovery sequence. In case the $\overline{\text{BKND_RECOVERY}}$ pin is pulled low, this register determines if this channel is to follow the error recovery sequence or to continue with no interruption.
D6	Determines if the power stage needs the TAS5508A VALID pin to go low to reset the power stage. Some power stages can be reset by a combination of PWM signals. For these devices, it is recommended to set this bit low, since the VALID pin is shared for power stages. This provides better control of each power stage.
D5	Determines if the power stage needs the TAS5508A VALID pin to go low to mute the power stage. Some power stages can be muted by a combination of PWM signals. For these devices, it is recommended to set this bit low, since the VALID pin is shared for power stages. This provides better control of each power stage.
D4	Inverts the PWM output. Inverting the PWM output can be an advantage if the power stage input pin are opposite the TAS5508A PWM pinout. This makes routing on the PCB easier. To keep the phase of the output the speaker terminals must also be inverted.
D3	The power stage TAS5182 has a special PWM input. To ensure that the TAS5508A has full control in all occasions, the PWM output must be remapped.
D2	Can be used to handle click and pop for some applications.
D1	This bit is normally used together with D2. For some power stages, both PWM signals must be high to get the desired operation of both speaker outputs to be low. This bit sets the PWM outputs high-high during mute.
D0	Not used

Table 2−6 lists the optimal setting for each output stage configuration. Note that the default value is applicable in all configurations except the TAS5182 SE/BTL configuration.

Table 2−6. Recommended TAS5508A Configurations for Texas Instruments Power Stages

DEVICE	ERROR RECOVERY	CONFIGURATION	D7	D6	D5	D4	D3	D2	D1	D0
Default	**RES**	**BTL**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**
TAS5111	RES	BTL	1	1	1	0	0	0	0	0
		SE	1	1	1	0	0	0	0	0
	AUT	BTL	0	1	1	0	0	0	0	0
		SE	0	1	1	0	0	0	0	0
TAS5112	RES	BTL	1	1	0	0	0	0	0	0
		SE	1	1	0	0	0	0	0	0
	AUT	BTL	0	1	0	0	0	0	0	0
		SE	0	1	0	0	0	0	0	0
TAS5182	RES	BTL	1	1	1	0	1	0	0	0
		SE	1	1	1	0	1	0	0	0

RES: The output stage requires $\overline{\text{VALID}}$ to go low to recover from a shutdown.

AUT: The power stage can auto recover from a shutdown.

BTL: Bridge tied load configuration

SE: Single-ended configuration

2.3.2 Headphone Configuration Registers

The headphone configuration controls are identical to the speaker configuration controls. The headphone configuration control settings are used in place of the speaker configuration control settings for channels 1 and 2 when the headphones are selected. In reality however, there is only one used configuration setting for headphones and that is the default setting.

2.3.3 Audio System Configurations

The TAS5508A can be configured to comply with various audio systems: 5.1-channel system, 6-channel system, 7.1-channel system and 8-channel system.

The audio system configuration is set in the General Control Register (0xE0). Bits D31 − D4 must be zero and D0 is don't care.

D3 Determines if SUB is to be controlled by PSVC (D3 is a write-only bit)

D2 Enable/Disable power supply volume control

D1 Sets number of speakers in the system, including possible line outputs

D3−D1 must be configured as the following according to the audio system in the application:

Table 2−7. Audio System Configuration (General Control Register 0xE0)

AUDIO SYSTEM	D31−D4	D3	D2	D1	D0
DEFAULT	**0**	**0**	**0**	**0**	**X**
6 channel or 5.1 NOT using PSVC	0	0	0	1	X
6 channel using PSVC	0	0	1	1	X
5.1 system using PSVC	0	1	1	1	X
8 channel or 7.1 NOT using PSVC	0	0	0	0	X
8 channel using PSVC	0	0	1	0	X
7.1 system using PSVC	0	1	1	0	X

2.3.3.1 Using Line Outputs in 6-Channel Configurations

The audio system can be configured for a 6-channel configuration (with 2 line outs) by writing a 1 to bit D1 of register 0xE0 (general control register). In this configuration, channel 5 and 6 processing are exactly the same as the other channels, except that master volume and the loudness function have no effect on the signal.

Note that in 6-channel configuration, channels 5 and 6 are unaffected by backend error ($\overline{\text{BKND_ERR}}$ goes low).

To use channels 5 and 6 as dry unprocessed line outs, the following setup is recommended:

- Channel 5 volume and channel 6 volume should be set for a constant output such as 0 dB.
- Bass and treble for channels 5 and 6 can be used if desired.
- DRC1 should be bypassed for channels 5 and 6.
- If a down mix is desired on the channel 5 and 6 as line out, the down mixing can be performed using the channel 5 and channel 6 input mixers.
- The operation of the channel 5 and 6 biquads is unaffected by the 6/8 channel configuration setting.

2.3.4 Recovery from Clock Error

The TAS5508A can be set to either perform a volume ramp up during the recovery sequence of a clock error or to simply come up in the last state (or desired state if a volume or tone update was in progress). This feature is enabled via I^2C system control register 0x03.

2.3.5 Power Supply Volume Control Enable

The power supply volume control (PSVC) can be enabled and disabled via I^2C register 0xE0. The subwoofer PWM output can configured to be controlled by the PSVC or digitally attenuated when PSVC is enabled (for powered subwoofer configurations). Note that PSVC cannot be simultaneously enabled along with unmute outputs after clock error feature.

2.3.6 Volume and Mute Update Rate

The TAS5508A has fixed soft volume and mute ramp durations. The ramps are linear. The soft volume and mute ramp rates are adjustable by programming the I^2C register 0xD0 for the appropriate number of steps to be 512, 1024, or 2048. The update is performed at a fixed rate regardless of the sample rate.

- In normal speed, the update rate is 1 step every 4 / Fs seconds.
- In double speed, the update is 1 step every 8 / Fs seconds.
- In quad speed, the update is 1 step every 16 / Fs seconds.

Because of processor loading, the update rate can increase for some increments by +1/Fs to +3/Fs. However, the variance of the total time to go from +18 dB to mute is less than 25%.

Table 2–8. Volume Ramp Rates in ms

NUMBER OF STEPS	SAMPLE RATE (KHZ)	
	44.1, 88.2, 176.4	32, 48, 96, 192
512	46.44 ms	42.67 ms
1024	92.88 ms	85.33 ms
2048	185.76 ms	170.67 ms

2.3.7 Modulation Index Limit

PWM modulation is a linear function of the audio signal. When the audio signal is 0, the PWM modulation is 50%. When the audio signal increases towards full scale, the PWM modulation increases towards 100%. For negative signals, the PWM modulations fall below 50% towards 0%.

However, there is a limit to the maximum modulation possible. During the off-time period, the power stage connected to the TAS5508A output needs to get ready for he next on-time period. The maximum possible modulation is then set by the power stage requirements. All Texas Instruments power stages needs maximum modulation to be 97.7%. This is also the default setting of the TAS5508A. Default settings can be changed in the Modulation Index Register (0x16).

Note that no change should be made to this register when using Texas Instruments power stages.

2.3.8 Inter-channel Delay

An 8-bit value can be programmed to each of the eight PWM inter-channel delay registers to add a delay per channel from 0 to 255 clock cycles. The delays correspond to cycles of the high-speed internal clock, DCLK. The default values are shown in Table 2−9.

Table 2−9. Inter-Channel Delay Default Values

I²C SUB-ADDRESS	CHANNEL	INTER-CHANNEL DELAY DEFAULT (DCLK PERIODS)
0x1B	1	−24
0x1C	2	0
0x1D	3	−16
0x1E	4	+16
0x1F	5	−24
0x20	6	+8
0x21	7	−8
0x22	8	+24

This delay is generated in the PWM and can be changed at any time through the serial control interface I²C registers 0x1B − 0x22. The absolute offset for channel 1 is set in I²C sub-address 0x23.

NOTE: If used correctly, setting the PWM channel delay can optimize the performance of a pure path digital amplifier system. The setting is based upon the type of backend power device that is used and the layout. These values are set during initialization using the I²C serial interface. Unless otherwise noted, use the default values given in Table 2−9.

2.4 Master Clock and Serial Data Rate Controls

The TAS5508A function only as a receiver of the MCLK (master clock), SCLK (shift clock), and LRCLK (left/right clock) signals that controls the flow of data on the four serial data interfaces. The 13.5-MHz external crystal allows the TAS5508A to automatically detect MCLK and the data rate.

The MCLK frequency can be 64 x Fs, 128 x Fs, 196 x Fs, 256 x Fs, 384 x Fs, 512 x Fs, or 768 x Fs.

The TAS5508A operates with the serial data interface signals LRCLK and SCLK synchronized to MCLK. However, there is no constraint as to the phase relationship of these signals. The TAS5508A accepts a 64 x Fs SCLK rate and a 1 x Fs LRCLK.

If the phase of SCLK or LRCLK drifts more than ±10 MCLK cycles since the last RESET, the TAS5508A performs a clock error and resynchronize the clock timing.

The clock and serial data interface have several control parameters:

- MCLK Ratio 64 Fs, 128 Fs, 196 Fs, 256 Fs, 384 Fs, 512 Fs, or 768 Fs) − I²C parameter
- Data Rate 32, 38, 44.1,48, 88.2, 96, 176.4, 192 kHz − I²C parameter
- AM Mode Enable / Disable − I²C parameter

During AM interference avoidance, the clock control circuitry utilizes three other configuration inputs:

- Tuned AM Frequency (for AM interference avoidance) (550 − 1750 kHz) − I²C parameter
- Frequency Set Select (1−4) − I²C parameter
- Sample Rate − I²C parameter or auto detected

2.4.1 PLL Operation

The TAS5508A uses two internal clocks generated by two internal phase-locked loops (PLLs), the digital PLL (DPLL) and the analog PLL (APLL). The analog PLL provides the reference clock for the PWM. The digital PLL provides the reference clock for the digital audio processor and the control logic.

The master clock MCLK input provides the input reference clock for the APLL. The external 13.5-MHz crystal provides the input reference clock for the digital PLL. The crystal provides a time base to support a number of operations, including the detection of the MCLK ratio, the data rate, and clock error conditions. The crystal time base provides a constant rate for all controls and signal timing.

Even if MCLK is not present, the TAS5508A can receive and store I^2C commands and provide status.

2.5 Bank Controls

The TAS5508A permits the user to specify and assign sample rate dependent parameters for Biquad, Loudness, DRC, and Tone in one of three banks that can be manually selected or selected automatically based upon the data sample rate. Each bank can be enabled for one or more specific sample rates via I^2C bank control register 0x40. Each bank set holds the following values:

- Coefficients for Seven Biquads (7X5 = 35 coefficients) for Each of the Eight Channels (Registers 0X51 – 0x88)
- Coefficients for One Loudness Biquad (Register 0x95)
- DRC1 Energy and (1 – Energy) Values (Register 0x98)
- DRC1 Attack, (1 – Attack), Decay, (1 – Decay) Values (Register 0x9C)
- DRC2 Energy and (1 – Energy) Values (Register 0x9D)
- DRC2 Attack, (1 – Attack), Decay, (1 – Decay) Values (Register 0xA1)
- Five Bass Filter-Set Selections (Register 0xDA)
- Five Treble Filter-Set Selections (Register 0xDC)

The default selection for bank control is manual bank with bank 1 selected. Note that if bank switching is used, Bank 2 and Bank 3 must be programmed on power–up since the default values are all zeroes. If bank switching is used and Bank 2 and Bank 3 are not programmed correctly, then the output of the TAS5508A could be muted when switching to those banks.

2.5.1 Manual Bank Selection

The three bank selection bits of the bank control register allow the appropriate bank to be manually selected (000 = Bank 1, 001 = Bank 2, 010 = Bank 3). In the manual mode, when a write occurs to the Biquad, DRC, or Loudness coefficients, the current selected bank is updated. If audio data is streaming to the TAS5508A, during a manual bank selection, the TAS5508A first performs a mute sequence, then performs the bank switch, and finally restores the volume using an un–mute sequence.

A mute command initiated by the bank switch mute sequence overrides an un–mute command or a volume command. While a mute is active, the commanded channels are muted. When a channel is unmated, the volume level goes to the last commanded volume setting that has been received for that channel.

If MCLK or SCLK is stopped, the TAS5508A performs a bank switch operation. If the clocks should start up once the manual bank switch command has been received, the bank switch operation is performed during the 5–ms silent start sequence.

2.5.2 Automatic Bank Selection

To enable automatic bank selection, a value of 3 is written into in the bank selection bits of the bank control register. Banks are associated with one or more sample rates by writing values into the Bank 1 or Bank 2 data rate selection registers. The automatic base selection is performed when a frequency change is detected according to the following scheme:

1. The system scans Bank 1 data rate associations to see if the Bank 1 is assigned for that data rate.
2. If Bank 1 is assigned, then the Bank 1 coefficients will be loaded.
3. If it is not then, the system scans the bank 2 to see if Bank 1 is assigned for that data rate.
4. If Bank 2 is assigned, then the Bank 2 coefficients will be loaded.
5. If it is not then, the system loads the Bank 3 coefficients.

The default is that all frequencies are enabled for Bank 1. This default is expressed as a value of all 1s in the Bank 1 auto-selection byte and all 0s in the bank 2 auto−section byte.

2.5.2.1 Coefficients Write Operations While Automatic Bank Switch Is Enabled

In automatic mode if a write occurs to the Tone, EQ, DRC, or Loudness coefficients, the bank that is written to is the current bank.

2.5.3 Bank Set

Bank set is used to provide a secure way to update the bank coefficients in both the manual and automatic switching modes without causing a bank switch to occur. Bank set mode does not alter the current bank register mapping. It simply enables any bank's coefficients to be updated while inhibiting any bank switches from taking place. In manual mode, this enables the coefficients to be set without switching banks. In automatic mode this prevents a clock error or data rate change from corrupting a bank coefficient write.

To update the coefficients of a bank, a value of 4, 5, or 6 is written into in the bank selection bits of the bank control register. This enables the Tone, EQ, DRC, and Loudness coefficient values of bank 1, 2, or 3 to be respectively updated.

Once the coefficients of the bank have been updated, the bank selection bits are then returned to the desired manual or automatic bank selection mode.

2.5.4 Bank Switch Timeline

After a bank switch is initiated (manual or automatic), no I^2C writes to the TAS5508A should occur before a minimum of 186 ms. This value is determined by the volume ramp rates for a particular sample rate.

2.5.5 Bank Switching Example 1

Problem: The audio unit containing a TAS5508A needs to handle different audio formats with different sample rates. Format #1 requires Fs = 32 kHz, Format #2 requires Fs = 44.1 kHz, and Format #3 requires Fs = 48 kHz. The sample-rate dependent parameters in the TAS5508A require different coefficients and data depending on the sample rate.

Strategy: Use the TAS5508A bank switching feature to allow for managing and switching three banks associated with the three sample rates, 32 kHz (Bank 1), 44.1 kHz (Bank 2), and 48 kHz (Bank 3).

One possible algorithm is to generate, load, and automatically manage bank switching for this problem:

- Generate bank-related coefficients (see above) for sample rates 32 kHz, 44.1 kHz, and 48 kHz and include the same in the micro-based TAS5508A I^2C firmware.
- On TAS5508A power up or reset, the micro runs the following TAS5508A Initialization code:
  - Update Bank 1 (Write 0x00048040 to register 0x40).
  - Write bank-related I^2C registers with appropriate values for Bank 1.
  - Write Bank 2 (Write 0x00058040 to register 0x40).
  - Load bank-related I^2C registers with appropriate values for Bank 2.
  - Write Bank 3 (Write 0x00068040 to register 0x40).
  - Load bank-related I^2C registers with appropriate values for Bank 3.
  - Select automatic bank switching (write 0x00038040 to register 0x40)

- Now when the audio media changes, the TAS5508A automatically detects the incoming sample rate and automatically switches to the appropriate bank.

In this example any sample rates other then 32 kHz and 44.1 kHz will use Bank 3. If other sample rates are used, then the banks need to be set−up differently.

2.5.6 Bank Switching Example 2

Problem: The audio system uses all of the sample rates supported by the TAS5508A. How can the automatic bank switching be set up to handle this situation?

Strategy: Use the TAS5508A bank switching feature to allow for managing and switching three banks associated with sample rates as follows:

- Bank 1: Coefficients for 32 kHz, 38 kHz, 44.1 kHz, and 48 kHz
- Bank 2: Coefficients for 88.2kHz and 96 kHz
- Bank 3: Coefficients for 176.4 kHz and 192 kHz

One possible algorithm is to generate, load, and automatically manage bank switching for this problem:

- Generate bank-related coefficients for sample rates 48 kHz (Bank 1), 96 kHz (Bank 2), and 192 kHz (Bank 3) and include the same in the micro-based TAS5508A I^2C firmware.
- On TAS5508A power−up or reset, the micro runs the following TAS5508A Initialization code:
  - Update Bank 1 (Write 0x0004F00C to register 0x40).
  - Write bank-related I^2C registers with appropriate values for Bank 1.
  - Write Bank 2 (Write 0x0005F00C to register 0x40).
  - Load bank-related I^2C registers with appropriate values for Bank 2.
  - Write Bank 3 (Write 0x0006F00C to register 0x40).
  - Load bank-related I^2C registers with appropriate values for Bank 3.
  - Select automatic bank switching (Write 0x0003F00C to register 0x40)
- Now when the audio media changes, the TAS5508A automatically detects the incoming sample rate and automatically switches to the appropriate bank.

3 Electrical Specifications

3.1 Absolute Maximum Ratings†

		UNITS
Supply voltage, DVDD and DVD_PWM		–0.3 V to 3.6 V
Supply voltage, AVDD_PLL		–0.3 V to 3.6 V
Input voltage	3.3-V digital input	–0.5 V to DVDD + 0.5 V
	5 V tolerant(2) digital input	–0.5 V to 6 V
	1.8 V LVCMOS(3)	–0.5 V to VREF(1) + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > 1.8 V		±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > 1.8 V)		±20 mA
Operating free air temperature		0°C to 70°C
Storage temperature range, T_{stg}		–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. VREF is a 1.8-V supply derived from regulators internal to the TAS5508A chip. VREF is on terminals VRA_PLL, VRD_PLL, VR_DPLL, VR_DIG, and VR_PWM. These terminals are provided to permit use of external filter capacitors, but should not be used to source power to external devices.

2. 5-V tolerant inputs are $\overline{\text{RESET}}$, PDN, $\overline{\text{MUTE}}$, $\overline{\text{HP_SEL}}$, SCLK, LRCLK, MCLK, SDIN1, SDIN2, SDIN3, SDIN4, SDA, and SCL.

3. VRA_PLL, VRD_PLL, VR_DPLL, VR_DIG, VR_PWM

DISSIPATION RATING TABLE (High-k Board, 105°C Junction)

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING
PAG	1869 mW	23.36 mW/°C	818 mW

3.2 Dynamic Performance (At Recommended Operating Conditions at 25°C)

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNITS
Dynamic range	TAS5508A + TAS5111 A-weighted (Fs = 48 kHz)		102		dB
Total harmonic distortion	TAS5111 A at 1 W		0.1%		
	TAS5508A ouput		0.01%		
Frequency response	32-kHz to 96-kHz sample rates		±0.1		dB
	176.4, 192-kHz sample rates		±0.2		

3.3 Recommended Operating Conditions (over 0°C to 70°C)

		MIN	NOM	MAX	UNITS
Digital supply voltage, DVDD and DVDD_PWM		3	3.3	3.6	V
Analog supply voltage, AVDD_PLL		3	3.3	3.6	V
High-level input voltage, V_{IH}	3.3 V	2			V
	5-V tolerant(4)	2			
	1.8-V LVCMOS (XTL_IN)	1.26			
Low-level input voltage, V_{IL}	3.3 V			0.8	V
	5-V tolerant(4)			0.8	
	1.8-V (XTL_IN)			0.54	
Operating ambient air temperature range, T_A		0	25	70	°C
Operating junction temperature range, T_J		0		105	°C

NOTE 4: 5-V tolerant inputs are SDA, SCL, $\overline{\text{RESET}}$, PDN, $\overline{\text{MUTE}}$, $\overline{\text{HP_SEL}}$, SCLK, LRCLK, MCLK, SDIN1, SDIN2, SDIN3, and SDIN4.

3.4 Electrical Characteristics Over Recommended Operating Conditions (Unless Otherwise Noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{OH}	High-level output voltage	3.3 V TTL and 5 V[6] tolerant	I_{OH} = –4 mA	2.4			V
		1.8-V LVCMOS (XTL_OUT)	I_{OH} = – 0.55 mA	1.44			
V_{OL}	Low-level output voltage	3.3-V TTL and 5 V[6] tolerant	I_{OL} = 4 mA			0.5	V
		1.8-V LVCMOS (XTL_OUT)	I_{OL} = 0.75 mA			0.5	
I_{OZ}	High-impedance output current	3.3-V TTL				±20	µA
I_{IL}	Low-level input current	3.3-V TTL	$V_I = V_{IL}$			±1	µA
		1.8-V LVCMOS (XTL_IN)	$V_I = V_{IL}$			±1	
		5 V tolerant[5]	V_I = 0 V DVDD = 3 V			±1	
I_{IH}	High-level input current	3.3-V TTL	$V_I = V_{IH}$			±1	µA
		1.8-V LVCMOS (XTL_IN)	$V_I = V_{IH}$			±1	
		5 V tolerant[5]	V_I = 5.5 V DVDD = 3 V			±20	
I_{DD}	Input supply current	Digital supply voltage, DVDD	Fs = 48 kHz		140		mA
			Fs = 96 kHz		150		
			Fs = 192kHz		155		
			Power down		8		
		Analog supply voltage, AVDD	Normal		20		mA
			Power down		2		

NOTES: 5. 5-V tolerant inputs are SDA, SCL, $\overline{\text{RESET}}$, $\overline{\text{PDN}}$, $\overline{\text{MUTE}}$, $\overline{\text{HP_SEL}}$, SCLK, LRCLK, MCLK, SDIN1, SDIN2, SDIN3, and SDIN4.
6. 5-V tolerant outputs are SCL and SDA

3.5 PWM Operation at Recommended Operating Conditions Over 0°C to 70°C

PARAMETER	TEST CONDITIONS	MODE	VALUE	UNITS
Output sample rate 1X – 8 x over sampled	32-kHz data rate ±4%	12 x sample rate	384	kHz
	44.1-, 88.2-, 176.4-kHz data rate ±4%	8, 4, and 2 x sample rate	352.8	kHz
	48, 96, 192 kHz data rate ±4%	8, 4, and 2 x sample rate	384	kHz

3.6 Switching Characteristics

3.6.1 Clock Signals Over Recommended Operating Conditions (Unless Otherwise Noted)

3.6.1.1 PLL Input Parameters and External Filter Components†

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
f_{XTALI}	Frequency, XTAL IN	Only use 13.5-MHz crystal ≤1000 ppm		13.5		MHz
f_{MCLKI}	Frequency, MCLK (1 / t_{cyc2})		2		50	MHz
	MCLK duty cycle duty cycle		40%	50%	60%	
	MCLK minimum high time	≥2-V MCLK = 49.152 MHz, Within the min and max duty cycle constraints	5			ns
	MCLK minimum low time	≤0.8-V MCLK = 49.152 MHz, Within the min and max duty cycle constraints	5			ns
	LRCLK allowable drift before LRCLK reset				10	MCLKs
	External PLL filter cap C1	SMD 0603 Y5V		100		nF
	External PLL filter cap C2	SMD 0603 Y5V		10		nF
	External PLL filter resistor R	SMD 0603, metal film		200		Ω
	External VRA_PLL decoupling	SMD, Y5V		100		nF

See the TAS5508A *Example Application Schematic* section.

3.6.2 Serial Audio Port

3.6.2.1 Serial Audio Ports Slave Mode Over Recommended Operating Conditions (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
f_{SCLKIN}	Frequency, SCLK 64 x fs	C_L = 30 pF	2.048		12.288	MHz
t_{su1}	Setup time, LRCLK to SCLK rising edge		10			ns
t_{h1}	Hold time, LRCLK from SCLK rising edge		10			ns
t_{su2}	Setup time, SDIN to SCLK rising edge		10			ns
t_{h2}	Hold time, SDIN from SCLK rising edge		10			ns
	LRCLK frequency		32	48	192	kHz
	SCLK duty cycle		40%	50%	60%	
	LRCLK duty cycle		40%	50%	60%	
	SCLK rising edges between LRCLK rising edges		64		64	SCLK edges
	LRCLK clock edge with respect to the falling edge of SCLK		–1/4		1/4	SCLK period

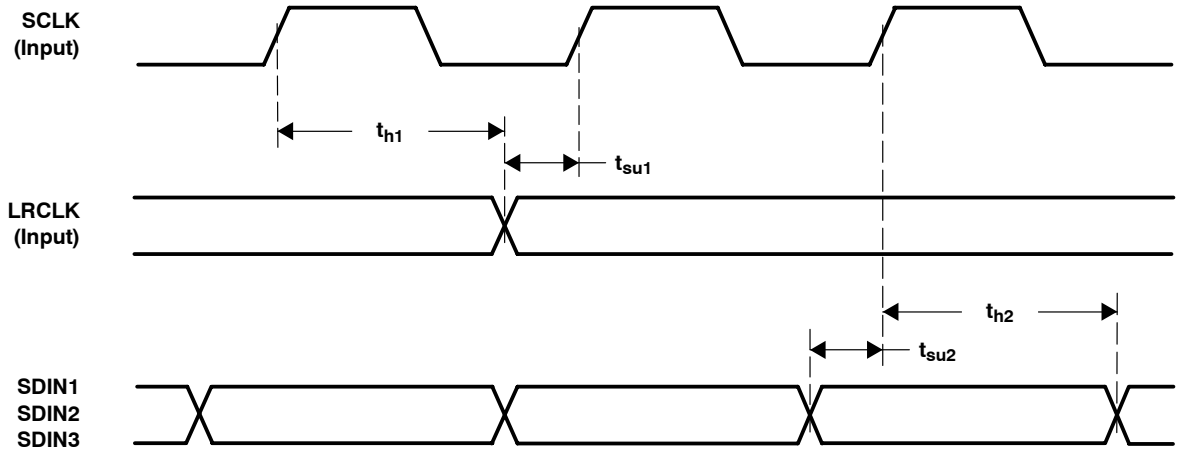


Figure 3–1. Slave Mode Serial Data Interface Timing

3.6.3 I²C Serial Control Port Operation

3.6.3.1 Timing Characteristics for I²C Interface Signals Over Recommended Operating Conditions (Unless Otherwise Noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNITS
f_{SCL}	Frequency, SCL	No wait states		400	kHz
$t_{w(H)}$	Pulse duration, SCL high		0.6		µs
$t_{w(L)}$	Pulse duration, SCL low		1.3		µs
t_r	Rise time, SCL and SDA			300	ns
t_f	Fall time, SCL and SDA			300	ns
t_{su1}	Setup time, SDA to SCL		100		ns
t_{h1}	Hold time, SCL to SDA		0		ns
$t_{(buf)}$	Bus free time between stop and start condition		1.3		µs
t_{su2}	Setup time, SCL to start condition		0.6		µs
t_{h2}	Hold time, start condition to SCL		0.6		µs
t_{su3}	Setup time, SCL to stop condition		0.6		µs
C_L	Load capacitance for each bus line			400	pF

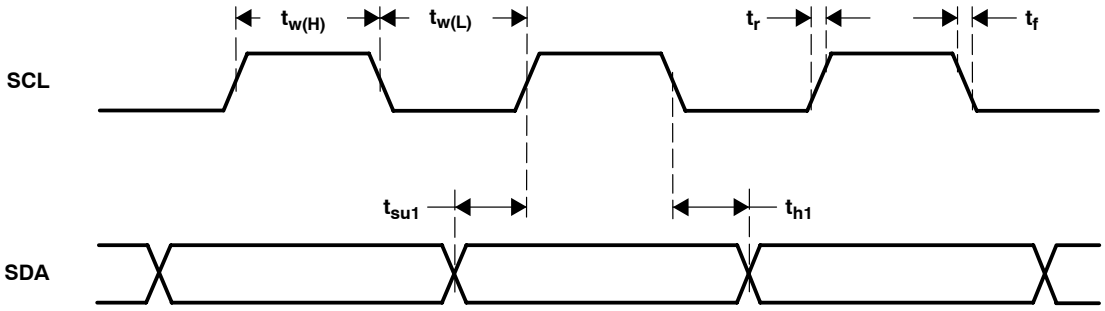


Figure 3–2. SCL and SDA Timing

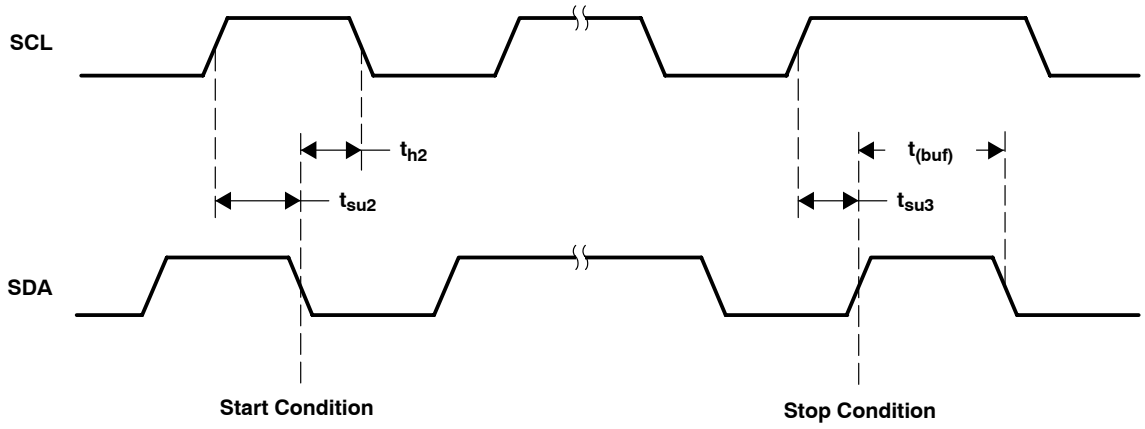


Figure 3–3. Start and Stop Conditions Timing

3.6.4 Reset Timing ($\overline{\text{RESET}}$)

3.6.4.1 Control Signal Parameters Over Recommended Operating Conditions (Unless Otherwise Noted)

PARAMETER		MIN	TYP	MAX	UNITS
$t_{r(DMSTATE)}$	Time to $\overline{\text{M-STATE}}$ low			370	ns
$t_{w(RESET)}$	Pulse duration, RESET active	400		None	ns
$t_{r(I2C_ready)}$	Time to enable I^2C		3		ms
$t_{r(run)}$	Device startup time	10			ms

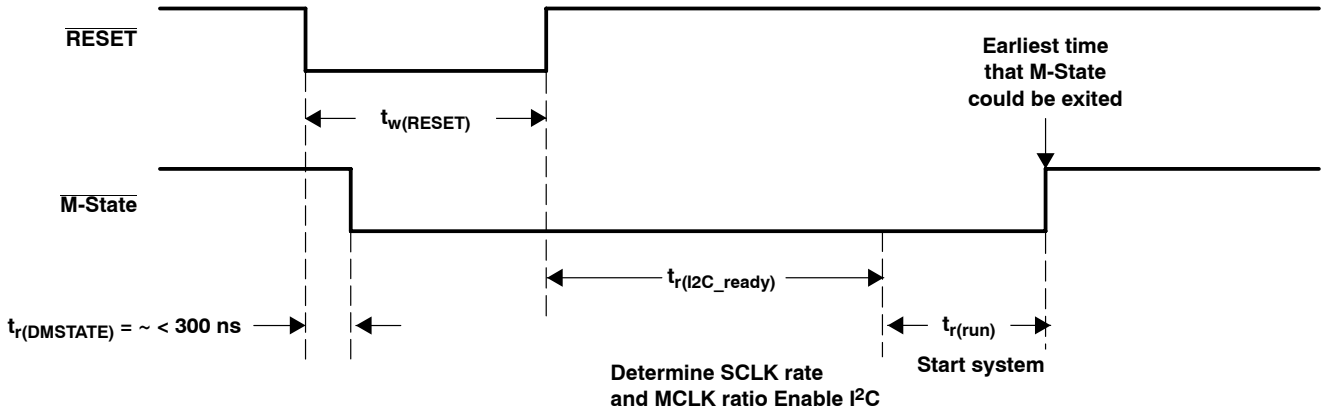


Figure 3–4. Reset Timing

Since a crystal time base is used, the system determines the CLK rates. Once the data rate and master clock ratio is determined, the system outputs audio if a master volume command is issued.

3.6.5 Power-Down ($\overline{\text{PDN}}$) Timing

3.6.5.1 Control Signal Parameters Over Recommended Operating Conditions (Unless Otherwise Noted)

PARAMETER		MIN	TYP	MAX	UNITS
$t_{p(DMSTATE)}$	Time to $\overline{\text{M-STATE}}$ low			300	μs
	Number of MCLKs preceding the release of $\overline{\text{PDN}}$	5			
t_{su}	Device startup time		120		ms

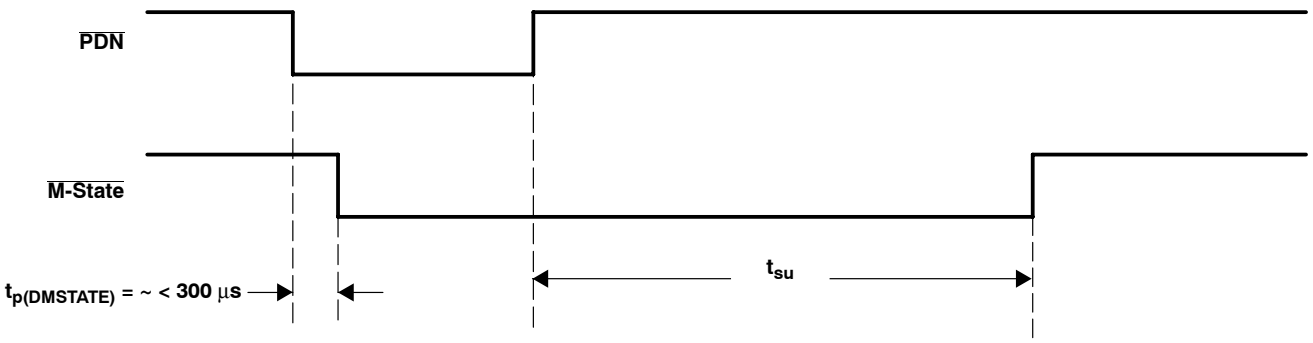


Figure 3–5. Power-Down Timing

3.6.6 Backend Error ($\overline{BKND_ERR}$)

3.6.6.1 Control Signal Parameters Over Recommended Operating Conditions (Unless Otherwise Noted)

PARAMETER		MIN	TYP	MAX	UNITS
$t_{w(ER)}$	Pulse duration, BKND_ERR active	350		None	ns
$t_{p(valid_low)}$				<100	µs
$t_{p(valid_high)}$	I^2C programmable to be between 1 to 10 ms	–25		25	% of interval

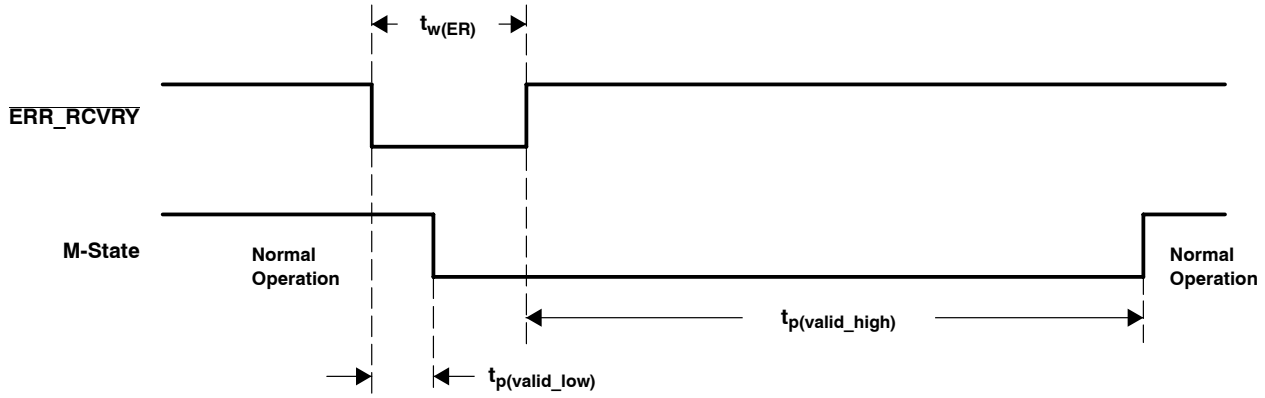


Figure 3–6. Error Recovery Timing

3.6.7 MUTE Timing—$\overline{MUTE}$

3.6.7.1 Control Signal Parameters Over Recommended Operating Conditions (Unless Otherwise Noted)

PARAMETER		MIN	TYP	MAX	UNITS
$t_{d(VOL}$	Volume ramp time	Defined by rate setting(1)			ms

NOTE 1: See the *Volume Treble and Base Slew Rate Register (0xD0)* section.

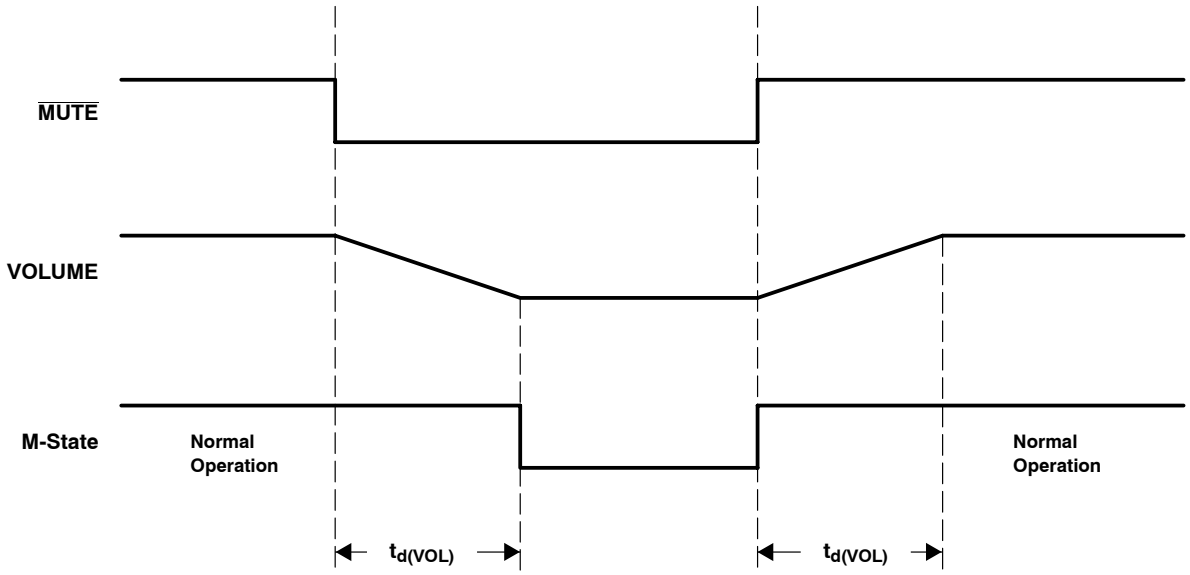


Figure 3–7. Mute Timing

3.6.8 *Headphone Select* (HP_SEL)

3.6.8.1 Control Signal Parameters Over Recommended Operating Conditions (Unless Otherwise Noted)

PARAMETER		MIN	MAX	UNITS
$t_{w(MUTE)}$	Pulse duration, HP_SEL active	350	None	ns
$t_{d(VOL)}$	Soft volume update time	Defined by rate setting(2)		ms
$t_{(SW)}$	Switch-over time	0.2	1 ms	ms

NOTE 2: See the *Volume Treble and Base Slew Rate Register (0xD0)* section.

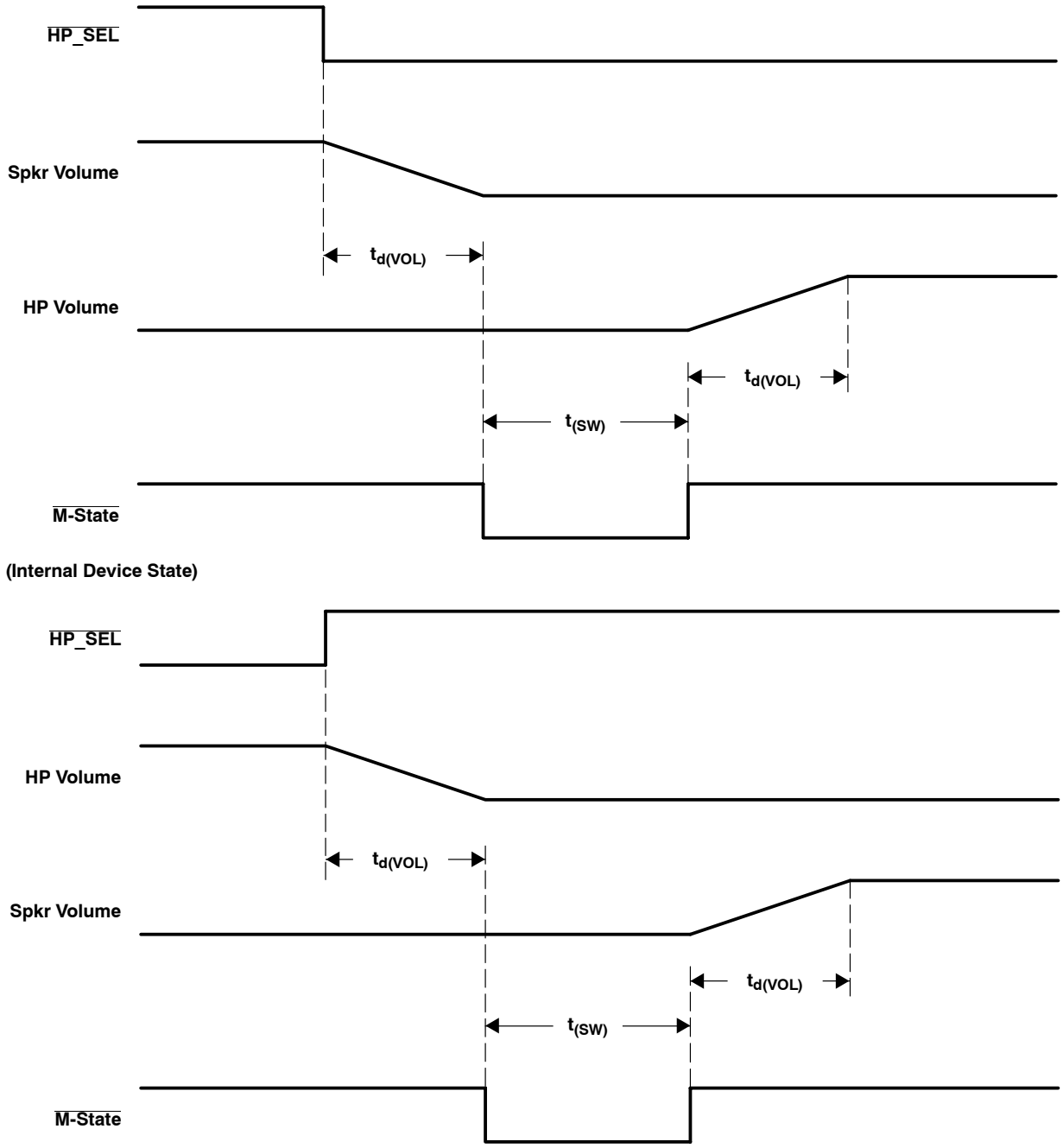


Figure 3–8. HP_SEL Timing

3.6.9 Volume Control

3.6.9.1 Control Signal Parameters Over Recommended Operating Conditions (Unless Otherwise Noted)

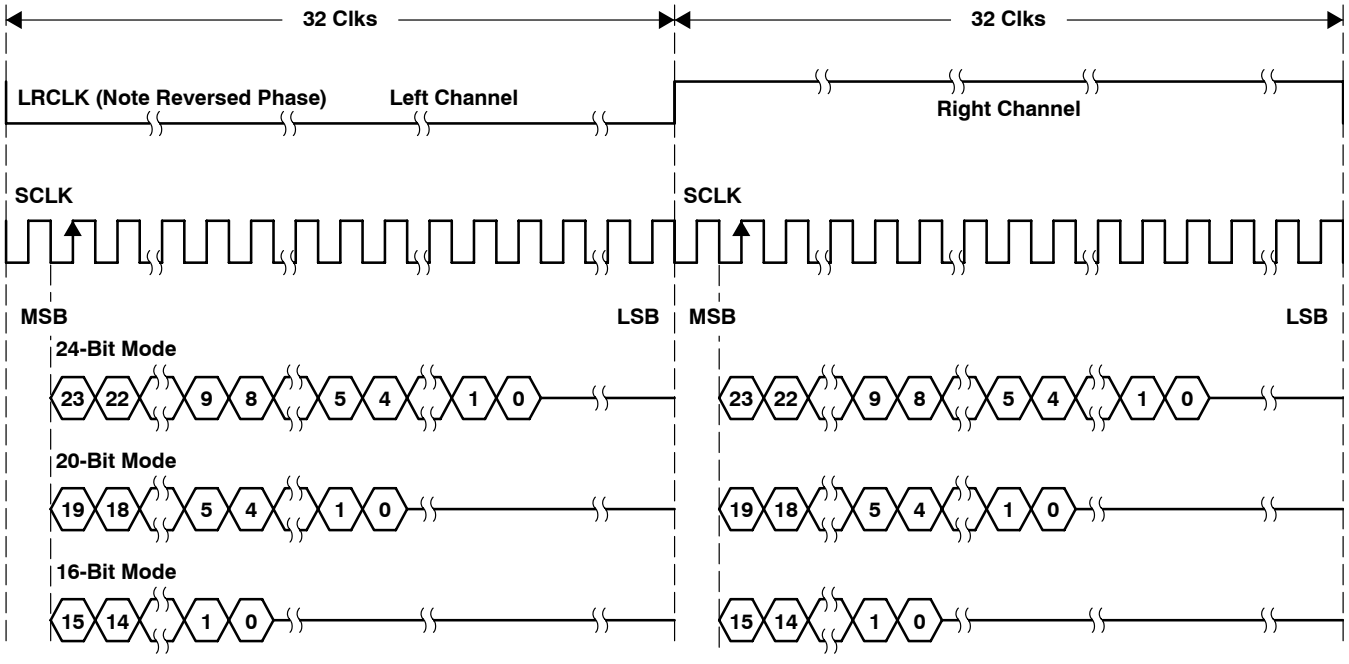
PARAMETER	TEST CONDITIONS	MIN	MAX	UNITS
Maximum attenuation before mute	Individual volume, master volume or a combination of both		−127	dB
Maximum gain	Individual volume, master volume		18	dB
Maximum volume before the onset of clipping	0-dB input, any modulation limit		0	dB
PSVC range	PSVC enabled	12, 18, or 24		dB
PSVC rate		Fs		
PSVC modulation		Single Sided		
PSVC quantization		2048		Steps
PSVC PWM modulation limits	PSVC range = 24 dB	6% (120 : 2048)	95% 1944 : 2048	dB

3.7 Serial Audio Interface Control and Timing

3.7.1 I²S Timing

I²S timing uses an LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. The LRCLK is low for the left channel and high for the right channel. A bit clock running at 64 × Fs is used to clock in the data. There is a delay of one bit clock from the time the LRCLK signal changes state to the first bit of data on the data lines. The data is written MSB first and is valid on the rising edge of bit clock. The TAS5508A masks unused trailing data bit positions.

2-Channel I²S (Philips Format) Stereo Input



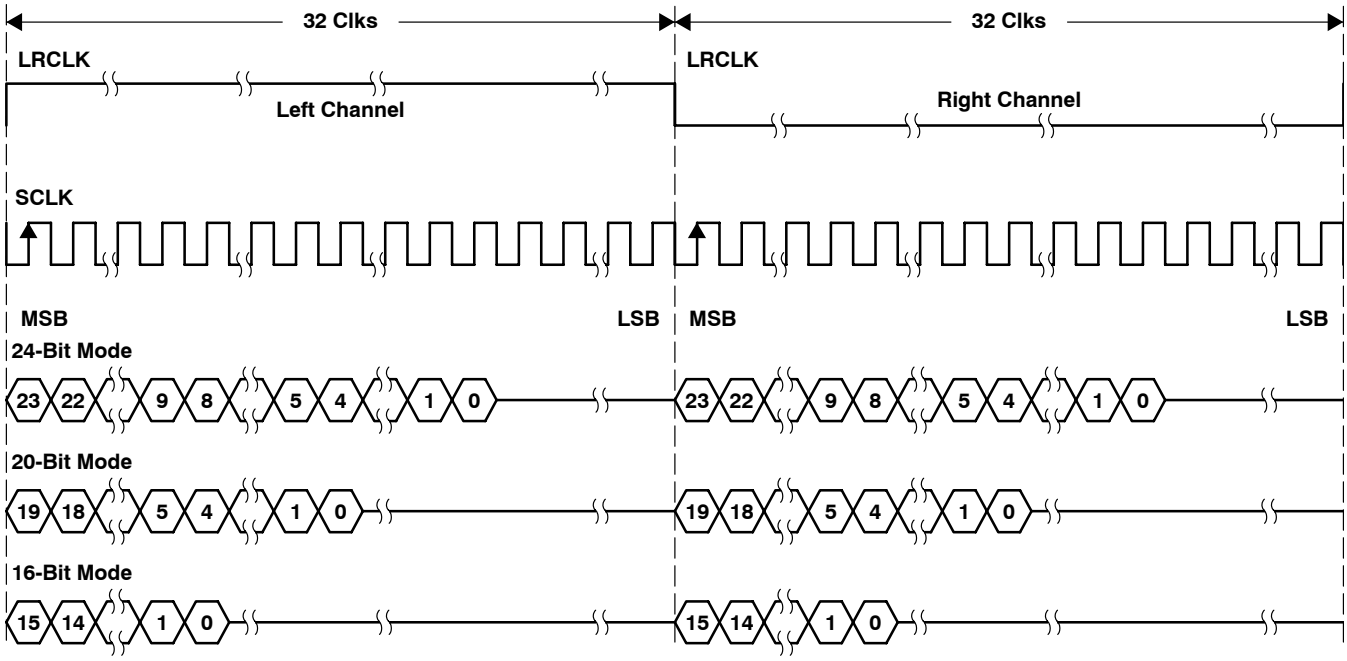
NOTE: All data presented in 2s complement form with MSB first.

Figure 3–9. I²S Format 64 Fs Format

3.7.2 Left Justified

Left justified (LJ) timing uses an LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. The LRCLK is high for the left channel and low for the right channel. A bit clock running at 64 × Fs is used to clock in the data. The first bit of data appears on the data lines at the same time the LRCLK toggles. The data is written MSB first and is valid on the rising edge of bit clock. The TAS5508A masks unused trailing data bit positions.

2-Channel Left-Justified Stereo Input



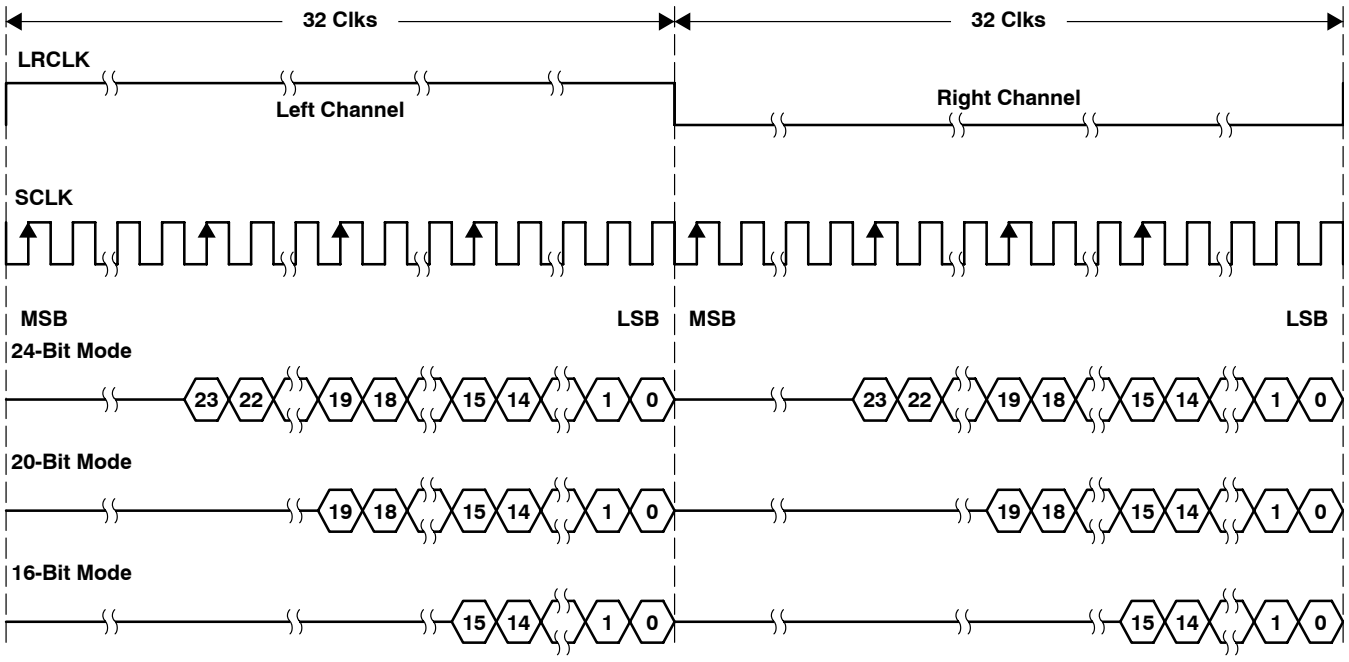
NOTE: All data presented in 2s complement form with MSB first.

Figure 3–10. Left Justified 64 Fs Format

3.7.3 Right Justified

Right justified (RJ) timing uses an LRCLK to define when the data being transmitted is for the left channel and when it is for the right channel. The LRCLK is high for the left channel and low for the right channel. A bit clock running at 64 × Fs is used to clock in the data. The first bit of data appears on the data 8-bit clock periods (for 24-bit data) after LRCLK toggles. In RJ mode the LSB of data is always clocked by the last bit clock before L/RCLK transitions. The data is written MSB first and is valid on the rising edge of bit clock. The TAS5508A masks unused leading data bit positions.

2-Channel Right-Justified (Sony Format) Stereo Input



NOTE: All data presented in 2s complement form with MSB first.

Figure 3–11. Right Justified 64 Fs Format

4 I²C Serial Control Interface (Slave Address 0x36)

The TAS5508A has a bidirectional I²C interface that compatible with the I²C (Inter IC) bus protocol and supports both 100 Kbps and 400 Kbps data transfer rates for single and multiple byte write and read operations. This is a slave only device that does not support a multi-master bus environment or wait state insertion. The control interface is used to program the registers of the device and to read device status.

The TAS5508A supports the standard-mode I²C bus operation (100 kHz maximum) and the fast I²C bus operation (400 kHz maximum). The TAS5508A performs all I²C operations without I²C wait cycles.

4.1 General I²C Operation

The I²C bus employs two signals; SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Data is transferred on the bus serially one bit at a time. The address and data can be transferred in byte (8-bit) format, with the most significant bit (MSB) transferred first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is high to indicate a start and stop conditions. A high-to-low transition on SDA indicates a start and a low-to-high transition indicates a stop. Normal data bit transitions must occur within the low time of the clock period. These conditions are shown in Figure 4–1. The master generates the 7-bit slave address and the read/write (R/W) bit to open communication with another device and then wait for an acknowledge condition. The TAS5508A holds SDA low during acknowledge clock period to indicate an acknowledgement. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/W bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection. An external pullup resistor must be used for the SDA and SCL signals to set the high level for the bus.

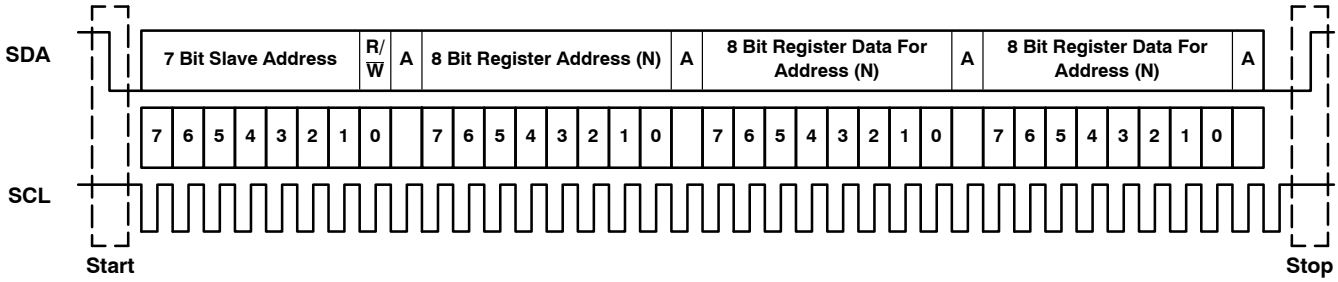


Figure 4–1. Typical I²C Sequence

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. A generic data transfer sequence is shown in Figure 4–1.

The 7-bit address for the TAS5508A is 0011011.

4.2 Single and Multiple Byte Transfers

The serial control interface supports both single-byte and multiple-byte read / write operations for status registers and the general control registers associated with the PWM. However, for the DAP data processing registers, the serial control interface supports only multiple byte (4 byte) read / write operations.

During multiple byte read operations, the TAS5508A responds with data, a byte at a time, starting at the subaddress assigned, as long as the master device continues to respond with acknowledges. If a particular subaddress does not contain 32 bits, the unused bits are read as logic 0.

During multiple byte write operations, the TAS5508A compares the number of bytes transmitted to the number of bytes that are required for each specific sub address. If a write command is received for a biquad subaddress, the TAS5508A expects to receive five 32-bit words. If fewer than five 32-bit data words have been received when a stop command (or another start command) is received, the data received is discarded. Similarly, if a write command is received for a mixer coefficient, the TAS5508A expects to receive one 32-bit word.

Supplying a subaddress for each subaddress transaction is referred to as random I²C addressing. The TAS5508A also supports sequential I²C addressing. For write transactions, if a subaddress is issued followed by data for that subaddress and the fifteen subaddresses that follow, a sequential I²C write transaction has taken place, and the data for all 16 subaddresses is successfully received by the TAS5508A. For I²C sequential write transactions, the subaddress then serves as the start address and the amount of data subsequently transmitted, before a stop or start is transmitted, determines how many subaddresses are written. As was true for random addressing, sequential addressing requires that a complete set of data be transmitted. If only a partial set of data is written to the last subaddress, the data for the last subaddress is discarded. However, all other data written is accepted; just the incomplete data is discarded.

4.3 Single Byte Write

As shown in Figure 4–2, a single byte data write transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write data transfer, the read/write bit will be a 0. After receiving the correct I²C device address and the read/write bit, the TAS5508A device responds with an acknowledge bit. Next, the master transmits the address byte or bytes corresponding to the TAS5508A internal memory address being accessed. After receiving the address byte, the TAS5508A again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the TAS5508A again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single byte data write transfer.

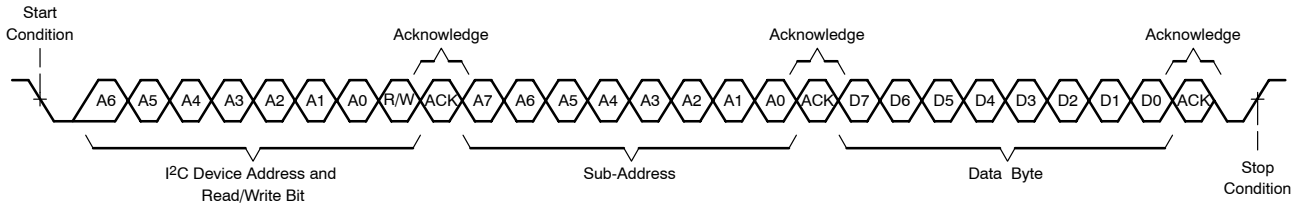


Figure 4–2. Single Byte Write Transfer

4.4 Multiple Byte Write

A multiple byte data write transfer is identical to a single byte data write transfer except that multiple data bytes are transmitted by the master device to TAS5508A as shown in Figure 4–3. After receiving each data byte, the TAS5508A responds with an acknowledge bit.

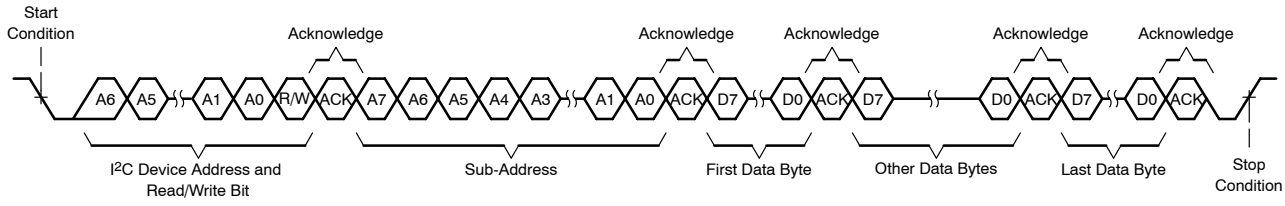


Figure 4–3. Multiple Byte Write Transfer

4.5 Incremental Multiple Byte Write

The I²C supports a special mode which permits I²C write operations to be broken up into multiple data write operations that are multiples of 4 data bytes. These are 6 byte, 10 byte, 14 byte, 18 byte, ... etc., write operations that are composed of a device address, read/write bit, and subaddress and any multiple of 4 bytes of data. This permits the system to incrementally write large register values without blocking other I²C transactions.

This feature is enabled by the append subaddress function in the TAS5508A. This function enables the TAS5508A to append 4 bytes of data to a register that was opened by a previous I²C register write operation but has not received its complete number of data bytes. Since the length of the long registers is a multiple of 4 bytes, using 4-byte transfers will have only an integer number of append operations.

When the correct number of bytes has been received, the TAS5508A starts processing the data.

The procedure to perform an incremental multi-byte write operation is as follows:

1. Start a normal I²C write operation by sending the device address, write bit, register subaddress, and the first four bytes of the data to be written. At the end of that sequence, send a stop condition. At this point, the register has been opened and accepts the remaining data that is sent by writing 4-byte blocks of data to the append subaddress (0xFE).
2. At a later time, one or more append data transfers are performed to incrementally transfer the remaining number of bytes in sequential order to complete the register write operation. Each of these append operations will be composed of the device address, write bit, append subaddress (0xFE), and four bytes of data followed by a stop condition.
3. The operation will be terminated due to an error condition and the data will be flushed:
   a. If a new subaddress is written to the TAS5508A before the correct number of bytes have been written.
   b. If more or less than 4 bytes are data written at the beginning or during any of the append operations.
   c. If a read bit is sent.

4.6 Single Byte Read

As shown in Figure 4–4, a single byte data read transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. For the data read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte or bytes of the internal memory address to be read. As a result, the read/write bit will be a 0. After receiving the TAS5508A address and the read/write bit, the TAS5508A responds with an acknowledge bit. In addition, after sending the internal memory address byte or bytes, the master device transmits another start condition followed by the TAS5508A address and the read/write bit again. This time the read/write bit will be a 1, indicating a read transfer. After receiving the TAS5508A and the read/write bit the TAS5508A again responds with an acknowledge bit. Next, the TAS5508A transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not acknowledge followed by a stop condition to complete the single byte data read transfer.

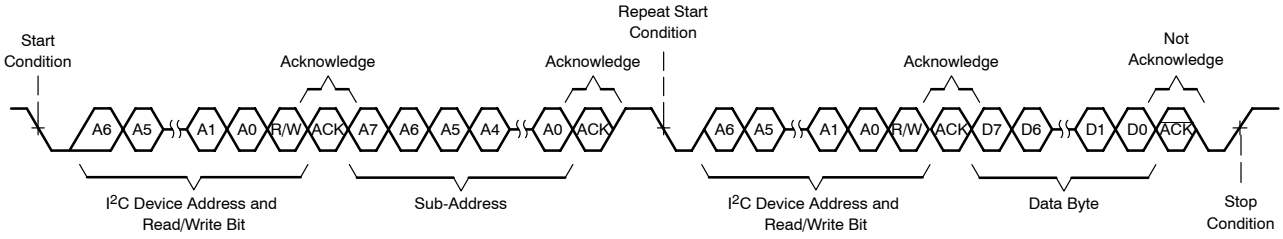


Figure 4–4. Single Byte Read Transfer

4.7 Multiple Byte Read

A multiple byte data read transfer is identical to a single byte data read transfer except that multiple data bytes are transmitted by the TAS5508A to the master device as shown in Figure 4–5. Except for the last data byte, the master device responds with an acknowledge bit after receiving each data byte.

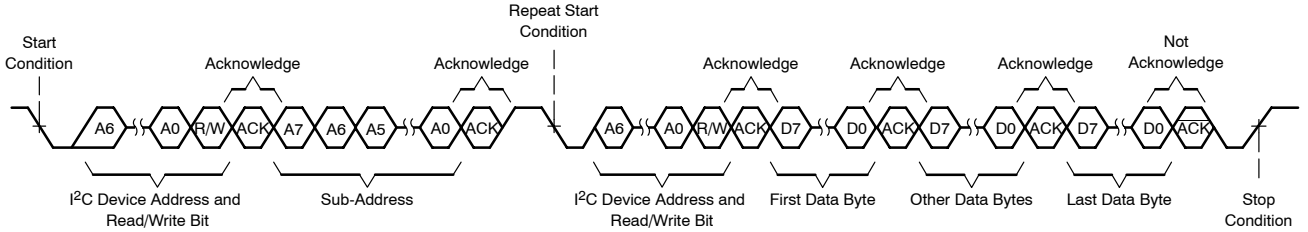


Figure 4–5. Multiple Byte Read Transfer

5 Serial Control I²C Register Summary

The TAS5508A slave address is 0x36. See the *Serial Control I²C Register Bit Definitions* chapter for complete bit definitions.

Note that u indicates unused bits.

I²C SUBADDRESS	TOTAL BYTES	REGISTER FIELDS	DESCRIPTION OF CONTENTS	DEFAULT STATE
0x00	1	Clock control register	Set data rate and MCLK frequency	1. Fs = 48 kHz 2. MCLK = 256 Fs = 12.288 MHz
0x01	1	General status register	Clip indicator and ID code for the TAS5508A	0x01
0x02	1	Error status register	PLL, SCLK, LRCLK, and frame slip errors	No errors
0x03	1	System control register 1	PWM high pass, clock set, un-mute select, PSVC select	1. PWM high pass disabled 2. Auto clock set 3. Hard un-mute on clock error recovery 4. PSVC HIZ disable
0x04	1	System control register 2	Automute and de-emphasis control	1. Automute timeout disable 2. Post-DAP detection automute enabled 3. 8-Ch device input detection automute enabled 4. Un-mute threshold 6 dB over input 5. No de-emphasis
0x05 – 0x0C	1	Channel configuration registers	Configure channels 1, 2, 3, 4, 5, 6, 7, and 8	1. Enable backend reset 2. Valid low for reset 3. Valid low for mute 4. Normal BEPolarity 5. Don't remap the output for the TAS5182 6. Don't go low-low in mute 7. Don't remap Hi-Z state to low-low state
0x0D	1	Headphone configuration register	Configure headphone output	1. Disable backend reset sequence 2 Valid does not have to be low for reset 3. Valid does not have to be low for mute 4. Normal BEPolarity 5. Don't remap output to comply with 5182 6. Don't go low-low in mute 7. Don't remap Hi–Z state to low-low state
0x0E	1	Serial data interface register	Set serial data interface to right justified, I2S, or left justified	24-bit I2S
0x0F	1	Soft mute register	Soft mute for channels 1, 2, 3, 4, 5, 6, 7, and 8	Un-mute all channels
0x10 – 0x13			RESERVED	
0x14	1	Automute control	Set auto-mute delay and threshold	1. Set auto-mute delay = 5 ms 2. Set auto-mute threshold less than bit 8
0x15	1	Automute PWM threshold and backend reset period	Set PWM auto-mute threshold, set backend reset period	1. Set the PWM threshold the same as the TAS5508A input threshold 2. Set backend reset period = 5 ms
0x16	1	Modulation limit register	Set modulation index	97.7%

I²C SUBADDRESS	TOTAL BYTES	REGISTER FIELDS	DESCRIPTION OF CONTENTS	DEFAULT STATE
0x17–0x1A			RESERVED	
0x1B–0x22	1/Reg.	Inter-channel delay registers	Set inter-channel delay	Channel 1 delay = –23 DCLK periods Channel 2 delay = 0 DCLK periods Channel 3 delay = –16 DCLK periods Channel 4 delay = +16 DCLK periods Channel 5 delay = –24 DCLK periods Channel 6 delay = 8 DCLK periods Channel 7 delay = –8 DCLK periods Channel 8 delay = 24 DCLK periods
0x23	1	Inter-channel offset	Absolute delay offset for channel 1 (0 – 255)	Minimum absolute default = 0 DCLK periods
0x24–0x3F			RESERVED	
0x40	4	Bank switching command register	Set up DAP coefficients bank switching for banks 1, 2, and 3	Manual selection – Bank 1
0x41–0x48	32/Reg	See the *Input Mixer Registers (0x41 – 0x48, Channels 1 – 8)* section	8X8 input crossbar mixer setup	SDIN1–Left to input mixer 1 SDIN1–Right to input mixer 2 SDIN2–Left to input mixer 3 SDIN2–Right to input mixer 4 SDIN3–Left to input mixer 5 SDIN3–Right to input mixer 6 SDIN4–Left to input mixer 7 SDIN4–Right to input mixer 8
0x49	4	ipmix_1_to_ch8	Input mixer 1 to Ch 8 mixer coefficient	0.0
0x4A	4	ipmix_2_to_ch8	Input mixer 1 to Ch 8 mixer coefficient	0.0
0x4B	4	ipmix_7_to_ch2	Input mixer 7 to Ch 2 mixer coefficient	0.0
0x4C	4	Ch7_bp_bq2	Bypass Ch 7 biquad 2 coefficient	0.0
0x4D	4	Ch7_bq2	Ch 7 biquad 2 coefficient	1.0
0x4E	4	ipmix_8_to_ch12	Ch 8 biquad 2 output to Ch1 mixer and Ch2 mixer coefficient	0.0
0x4F	4	Ch8_bp_bq2	Bypass Ch 8 biquad 2 coefficient 0	0.0
0x50	4	Ch8_bq2	Ch 8 biquad 2 coefficient	1.0
0x51–0x88	20/Reg.	See the next section	Channels 1, 2, 3, 4, 5, 6, 7, and 8 biquad filter coefficients	All biquads = All pass for all channels
0x89–0x90	8	Bass and Treble Bypass Ch 1 – 8	Bypass bass and treble for channels 1–8	Bass and treble bypassed for all channels
0x91	4	Loudness Log2 LG	Loudness Log2 LG	0.5
0x92	8	Loudness Log2 LO	Loudness Log2 LO	0.0
0x93	4	Loudness G	Loudness G	0.0
0x94	8	Loudness O	Loudness O	0.0
0x95	20	Loudness biquad	Loudness biquad coefficient b0	0x00, 0x00, 0xD5, 0x13
			Loudness biquad coefficient b1	0x00, 0x00, 0x00, 0x00
			Loudness biquad coefficient b2	0x0F, 0xFF, 0x2A, 0xED
			Loudness biquad coefficient a0	0x00, 0xFE, 0x50, 0x45
			Loudness biquad coefficient a1	0x0F, 0x81, 0xAA, 0x27
0x96	4	DRC1 control channels 1, 2, 3, 4, 5, 6, and 7	DRC1 control channels 1, 2, 3, 4, 5, 6, and 7	DRC1 disabled in channels 1, 2, 3, 4, 5, 6, and 7
0x97	4	DRC2 Ch 8 Control	DRC1 control channel 8	DRC2 disabled (channel 8)
0x98	8	Channels 1, 2, 3, 4, 5, 6, and 7, DRC1 energy	DRC1 energy	0.0041579
		Channels 1, 2, 3, 4, 5, 6, and 7, DRC1 (1– energy)	DRC1 (1 energy)	0.9958421

I²C SUBADDRESS	TOTAL BYTES	REGISTER FIELDS	DESCRIPTION OF CONTENTS	DEFAULT STATE
0x99	16	Channels 1, 2, 3, 4, 5, 6, and 7 DRC1 threshold T1	DRC1 threshold (T1) – upper 4 bytes	0x00, 0x00, 0x00, 0x00
			DRC1 threshold (T1) – lower 4 bytes	0x0B, 0x20, 0xE2, 0xB2
		Channels 1, 2, 3, 4, 5, 6, and 7 DRC1 thresholdT2	DRC1 threshold (T2) – upper 4 bytes	0x00, 0x00, 0x00, 0x00
			DRC1 threshold (T2) – lower 4 bytes	0x06, 0xF9, 0xDE, 0x58
0x9A	12	Channels 1, 2, 3, 4, 5, 6, and 7 , DRC1 slope k0	DRC1 slope (k0)	0x0F, 0xC0, 0x00, 0x00
		Channels 1, 2, 3, 4, 5, 6, and 7, DRC1 slope k1	DRC1 slope (k1)	0x0F, 0xC0, 0x00, 0x00
		Channels 1, 2, 3, 4, 5, 6, and 7 DRC1 slope k2	DRC1 slope (k2)	0x0F, 0x90, 0x00, 0x00
0x9B	16	Channels 1, 2, 3, 4, 5, 6, and 7 DRC1 offset 1	DRC1 offset 1 (O1) – upper 4 bytes	0x00, 0x00, 0xFF, 0xFF
			DRC1 offset 1 (O1) – lower 4 bytes	0xFF, 0x82, 0x30, 0x98
		Channels 1, 2, 3, 4, 5, 6, and 7 DRC1 offset 2	DRC1 offset 2 (O2) – upper 4 bytes	0x00, 0x00, 0x00, 0x00
			DRC1 offset 2 (O2) – lower 4 bytes	0x01, 0x95, 0xB2, 0xC0
0x9C	16	Channels 1, 2, 3, 4, 5, 6, and 7 DRC1 attack	DRC1 attack	0x00, 0x00, 0x88, 0x3F
		Channels 1, 2, 3, 4, 5, 6, and 7 DRC1 (1– Attack)	DRC1 (1 – Attack)	0x00, 0x7F, 0x77, 0xC0
		Channels 1, 2, 3, 4, 5, 6, and 7 DRC1 Delay	DRC1 delay	0x00, 0x00, 0x00, 0xAE
		Channels 1, 2, 3, 4, 5, 6, and 7 DRC1 (1– Delay)	DRC1 (1 – Delay)	0x00, 0x7F, 0xFF, 0x51
0x9D	8	Ch 8 DRC2 energy	DRC2 energy	0x00, 0x00, 0x88, 0x3F
		Ch 8 DRC2 (1– Energy)	DRC2 (1 – Energy)	0x00, 0x7F, 0x77, 0xC0
0x9E	16	CH 8 DRC2 threshold T1	DRC2 threshold (T1) – upper 4 bytes	0x00, 0x00, 0x00, 0x00
			DRC2 threshold (T1) – lower 4 bytes	0x0B, 0x20, 0xE2, 0xB2
		CH 8 DRC2 threshold T2	DRC2 threshold (T2) – upper 4 bytes	0x00, 0x00, 0x00, 0x00
			DRC2 threshold (T2) – lower 4 bytes	0x06, 0xF9, 0xDE, 0x58
0x9F	12	Ch 8 DRC2 slope k0	DRC2 slope (k0)	0x00, 0x40, 0x00, 0x00
		Ch 8 DRC2 slope k1	DRC2 slope (k1)	0x0F, 0xC0, 0x00, 0x00
		Ch 8 DRC2 slope k2	DRC2 slope (k2)	0x0F, 0x90, 0x00, 0x00
0xA0	16	Ch 8 DRC2 offset 1	DRC2 offset (O1) – upper 4 bytes	0x00, 0x00, 0xFF, 0xFF
			DRC2 offset (O1) – lower 4 bytes	0xFF, 0x82, 0x30, 0x98
		Ch 8 DRC2 offset 2	DRC2 offset (O2) – upper 4 bytes	0x00, 0x00, 0x00, 0x00
			DRC2 offset (O2) – lower 4 bytes	0x01, 0x95, 0xB2, 0xC0
0xA1	16	Ch 8 DRC2 attack	DRC 2 attack	0x00, 0x00, 0x88, 0x3F
		Ch 8 DRC2 (1– Attack)	DRC2 (1 – Attack)	0x00, 0x7F, 0x77, 0xC0
		Ch 8 DRC2 Delay	DRC2 delay	0x00, 0x00, 0x00, 0xAE
		Ch 8 DRC2 (1– Delay)	DRC2 (1 – Delay)	0x00, 0x7F, 0xFF, 0x51
0xA2	8	DRC bypass 1	Channel 1 DRC1 bypass coefficient	1.0
		DRC inline 1	Channel 1 DRC1 inline coefficient	0.0

I²C SUBADDRESS	TOTAL BYTES	REGISTER FIELDS	DESCRIPTION OF CONTENTS	DEFAULT STATE
0xA3	8	DRC bypass 2	Channel 2 DRC1 bypass coefficient	1.0
		DRC inline 2	Channel 2 DRC1 inline coefficient	0.0
0xA4	8	DRC bypass 3	Channel 3 DRC1 bypass coefficient	1.0
		DRC inline 3	Channel 3 DRC1 inline coefficient	0.0
0xA5	8	DRC bypass 4	Channel 4 DRC1 bypass coefficient	1.0
		DRC inline 4	Channel 4 DRC1 inline coefficient	0.0
0xA6	8	DRC bypass 5	Channel 5 DRC1 bypass coefficient	1.0
		DRC inline 5	Channel 5 DRC1 inline coefficient	0.0
0xA7	8	DRC bypass 6	Channel 6 DRC1 bypass coefficient	1.0
		DRC inline 6	Channel 6 DRC1 inline coefficient	0.0
0xA8	8	DRC bypass 7	Channel 7 DRC1 bypass coefficient	1.0
		DRC inline 7	Channel 7 DRC1 inline coefficient	0.0
0xA9	8	DRC bypass 8	Channel 8 DRC2 bypass coefficient	1.0
		DRC inline 8	Channel 8 DRC2 inline coefficient	0.0
0xAA	8	sel op1–8 and mix to S	Select 0 to 2 of eight channels to output mixer S	Select channel 1 to PWM 1
0xAB	8	sel op1–8 and mix to T	Select 0 to 2 of eight channels to output mixer T	Select channel 2 to PWM 2
0xAC	8	sel op1–8 and mix to U	Select 0 to 2 of eight channels to output mixer U	Select channel 3 to PWM 3
0xAD	8	sel op1–8 and mix to V	Select 0 to 2 of eight channels to output mixer V	Select channel 4 to PWM 4
0xAE	8	sel op1–8 and mix to W	Select 0 to 2 of eight channels to output mixer W	Select channel 5 to PWM 5
0xAF	8	sel op1–8 and mix to X	Select 0 to 2 of eight channels to output mixer X	Select channel 6 to PWM 6
0xB0	12	sel op1–8 and mix to Y	Select 0 to 3 of eight channels to output mixer Y	Select channel 7 to PWM 7
0xB1	12	sel op1–8 and mix to Z	Select 0 to 3 of eight channels to output mixer Z	Select channel 8 to PWM 8
0xB2–0xCE			RESERVED	
0xCF	20	Volume biquad	Volume biquad	All pass
0xD0	4	Vol, T and B slew rates	U (31:24), U (23:16), U (15:12) VSR(11:8), TBSR(7:0)	0x00, 0x00, 0x01, 0x3F
0xD1	4	Ch1 volume	Channel 1 volume	0 dB
0xD2	4	Ch2 volume	Channel 2 volume	0 dB
0xD3	4	Ch3 volume	Channel 3 volume	0 dB
0xD4	4	Ch4 volume	Channel 4 volume	0 dB
0xD5	4	Ch5 volume	Channel 5 volume	0 dB
0xD6	4	Ch6 volume	Channel 6 volume	0 dB
0xD7	4	Ch7 volume	Channel 7 volume	0 dB
0xD8	4	Ch8 volume	Channel 8 volume	0 dB
0xD9	4	Master volume	Master volume	Mute
OXDA	4	Bass filter set (1–5)	Bass filter set (all channels)	Filter set 3
0xDB	4	Bass filter index	Bass filter level (all channels)	0 dB
0xDC	4	Treble filter set (1–5)	Treble filter set (all channels)	Filter set 3
0xDD	4	Treble filter index	Treble filter level (all channels)	0 dB

I²C SUBADDRESS	TOTAL BYTES	REGISTER FIELDS	DESCRIPTION OF CONTENTS	DEFAULT STATE
0xDE	4	AM mode and tuned frequency register	Set-up AM mode for AM-interference reduction	AM mode disabled Select sequence 1 IF frequency = 455 kHz Use BCD-tuned frequency
0xDF	4	PSVC control range	Set PSVC control range	12-dB control range
0xE0	4	General control register	Six or eight channel configuration, PSVC enable	Eight channel configuration Power supply volume control disabled
0xE1–0xFD			RESERVED	
0xFE	4 (min)	Multiple byte write append register	Special register	N/A
0xFF			RESERVED	

6 Serial Control Interface Register Definitions

Unless otherwise noted, the I^2C register default values are in **bold** font.

Note that u indicates unused bits.

6.1 Clock Control Register (0x00)

Bit D1 is *Don't Care*.

Table 6–1. Clock Control Register

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	–	–	–		–	32-kHz data rate
0	0	1	–	–	–		–	38-kHz data rate
0	1	0	–	–	–		–	44.1-kHz data rate
0	**1**	**1**	**–**	**–**	**–**		**–**	**48-kHz data rate**
1	0	0	–	–	–		–	88.2-kHz data rate
1	0	1	–	–	–		–	96-kHz data rate
1	1	0	–	–	–		–	176.4-kHz data rate
1	1	1	–	–	–		–	192-kHz data rate
–	–	–	0	0	0			MCLK frequency = 64
–	–	–	0	0	1			MCLK frequency = 128
–	–	–	0	1	0			MCLK frequency = 192
–	**–**	**–**	**0**	**1**	**1**			**MCLK frequency = 256**
–	–	–	1	0	0			MCLK frequency = 384
–	–	–	1	0	1			MCLK frequency = 512
–	–	–	1	1	0			MCLK frequency = 768
–	–	–	1	1	1			Reserved
–	–	–	–	–	–		1	Clock register is valid (read only)
–	**–**	**–**	**–**	**–**	**–**		**0**	**Clock register is not valid (read only)**

6.2 General Status Register 0 (0x01)

Table 6–2. General Status Register (0x01)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
1	–	–	–	–	–	–	–	Clip indicator
–	1	–	–	–	–	–	–	Bank switching busy
–	**–**	**0**	**0**	**0**	**0**	**0**	**1**	**Identification code for TAS5508A**

6.3 Error Status Register (0x02)

Note that the error bits are sticky bits that are not cleared by the hardware. This means that the software must clear the register (write zeroes) and than read them to determine if there are any persistent errors.

Table 6–3. Error Status Register (0X02)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
1	–	–	–	–	–	–	–	PLL phase lock error
–	1	–	–	–	–	–	–	PLL auto lock error
–	–	1	–	–	–	–	–	SCLK error
–	–	–	1	–	–	–	–	LRCLK error
–	–	–	–	1	–	–	–	Frame slip
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	No errors

6.4 System Control Register 1 (0x03)

Bit D5, D2, D1, and D0 are *Don't Care*.

Table 6–4. System Control Register 1

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	**–**		**–**	**–**				**PWM high pass disabled**
1	–		–	–				PWM high pass enabled
–	–		0					Soft unmute on recovery from clock error
–	**–**		**1**					**Hard unmute on recovery from clock error**
–	–		–	1				PSVC Hi-Z enable
–	**–**		**–**	**0**				**PSVC Hi-Z disable**

6.5 System Control Register 2 (0x04)

Bit D3 and D2 are *Don't Care*.

Table 6–5. System Control Register 2

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	**–**	**–**	**–**			**–**	**–**	**Reserved**
–	**0**	**–**	**–**			**–**	**–**	**PWM automute detection enabled**
–	1	–	–			–	–	PWM automute detection disabled
		0	**–**			**–**	**–**	**8 Ch device input detection automute enabled**
–	–	1	–			–	–	8 Ch device input detection automute disabled
–	**–**	**–**	**0**			**–**	**–**	**Unmute threshold 6 dB over input threshold**
–	–	–	1			–	–	Unmute threshold equal to input threshold
–	**–**	**–**	**–**			**0**	**0**	**No de-emphasis**
–	–	–	–			0	1	De-emphasis for Fs = 32 kHz
–	–	–	–			1	0	De-emphasis for Fs = 44.1 kHz
–	–	–	–			1	1	De-emphasis for Fs = 48 kHz

6.6 Channel Configuration Control Register (0x05–X0C)

Channels 1, 2, 3, 4, 5, 6, 7, and 8 are mapped into 0x05, 0x06, 0x07, 0x08, 0x09, 0x0A, 0x0B, and 0x0C.

Bit D0 is *Don't Care*.

Table 6–6. Channel Configuration Control Registers

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	–	–	–	–	–	–		Disable backend reset sequence for a channel – BEErrorRecEn
1	**–**	**–**	**–**	**–**	**–**	**–**		**Enable backend reset sequence for a channel**
–	0	–	–	–	–	–		Valid does not have to be low for this channel to be reset BEValidRst
–	**1**	**–**	**–**	**–**	**–**	**–**		**Valid must be low for this channel to be reset**
–	–	0	–	–	–	–		Valid does not have to be low for this channel to be muted BEValidMute
–	**–**	**1**	**–**	**–**	**–**	**–**		**Valid must be low for this channel to be muted**
–	**–**	**–**	**0**	**–**	**–**	**–**		**Normal BEPolarity**
–	–	–	1	–	–	–		Switches PWM+ and PWM– and invert audio signal
–	**–**	**–**	**–**	**0**	**–**	**–**		**Do not remap output to comply with 5182 interface**
–	–	–	–	1	–	–		Remap output to comply with 5182 interface
–	**–**	**–**	**–**	**–**	**0**	**–**		**Do not go to low low in mute – BELowMute**
–	–	–	–	–	1	–		Go to low-low in Mute
–	**–**	**–**	**–**	**–**	**–**	**0**		**Do not remap Hi-Z state to low-low state – BE5111BsMute**
–	–	–	–	–	–	1		Remap Hi-Z state to low-low state

6.7 Headphone Configuration Control Register (0x0D)

Bit D0 is *Don't Care*.

Table 6–7. Headphone Configuration Control Register

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	–	–	–	–	–	–		**Disable backend reset sequence for a channel – BEErrorRecEn**
1	–	–	–	–	–	–		Enable backend reset sequence for a channel
–	**0**	**–**	**–**	**–**	**–**	**–**		**Valid does not have to be low for this channel to be reset BEValidRst**
–	1	–	–	–	–	–		Valid must be low for this channel to be reset
–	**–**	**0**	**–**	**–**	**–**	**–**		**Valid does not have to be low for this channel to be muted BEValidMute**
–	–	1	–	–	–	–		Valid must be low for this channel to be muted
–	**–**	**–**	**0**	**–**	**–**	**–**		**Normal BEPolarity**
–	–	–	1	–	–	–		Switches PWM+ and PWM– and invert audio signal
–	**–**	**–**	**–**	**0**	**–**	**–**		**Do not remap output to comply with 5182 interface**
–	–	–	–	1	–	–		Remap output to comply with 5182 interface
–	**–**	**–**	**–**	**–**	**0**	**–**		**Do not go to low low in mute – BELowMute**
–	–	–	–	–	1	–		Go to low-low in Mute
–	**–**	**–**	**–**	**–**	**–**	**0**		**Do not remap Hi-Z state to low-low state – BE5111BsMute**
–	–	–	–	–	–	1		Remap Hi-Z state to low-low state

6.8 Serial Data Interface Control Register (0x0E)

Nine serial modes can be programmed I^2C.

Table 6–8. Serial Data Interface Control Register Format

RECEIVE SERIAL DATA INTERFACE FORMAT	WORD LENGTHS	D7–D4	D3	D2	D1	D0
Right justified	16	0000	0	0	0	0
Right justified	20	0000	0	0	0	1
Right justified	24	0000	0	0	1	0
I^2S	16	0000	0	0	1	1
I^2S	20	0000	0	1	0	0
I^2S	**24**	0000	**0**	**1**	**0**	**1**
Left justified	16	0000	0	1	1	0
Left justified	20	0000	0	1	1	1
Left justified	24	0000	1	0	0	0
Illegal		0000	1	0	0	1
Illegal		0000	1	0	1	0
Illegal		0000	1	0	1	1
Illegal		0000	1	1	0	0
Illegal		0000	1	1	0	1
Illegal		0000	1	1	1	0
Illegal		0000	1	1	1	1

6.9 Soft Mute Register (0x0F)

Table 6–9. Soft Mute Register

D7	D6	D5	D4	D3	D2	D1	D0	Function
–	–	–	–	–	–	–	1	Soft Mute Channel 1
–	–	–	–	–	–	1	–	Soft Mute Channel 2
–	–	–	–	–	1	–	–	Soft Mute Channel 3
–	–	–	–	1	–	–	–	Soft Mute Channel 4
–	–	–	1	–	–	–	–	Soft Mute Channel 5
–	–	1	–	–	–	–	–	Soft Mute Channel 6
–	1	–	–	–	–	–	–	Soft Mute Channel 7
1	–	–	–	–	–	–	–	Soft Mute Channel 8
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Unmute All Channels**

6.10 Automute Control Register(0x14)

Table 6–10. Automute Control Register

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
–	–	–	–	0	0	0	0	Set input automute and PWM automute delay to 1 ms
–	–	–	–	0	0	0	1	Set input automute and PWM automute delay to 2 ms
–	–	–	–	0	0	1	0	Set input automute and PWM automute delay to 3 ms
–	–	–	–	0	0	1	1	Set input automute and PWM automute delay to 4 ms
–	**–**	**–**	**–**	**0**	**1**	**0**	**0**	**Set input automute and PWM automute delay to 5 ms**
–	–	–	–	0	1	0	1	Set input automute and PWM automute delay to 10 ms
–	–	–	–	0	1	1	0	Set input automute and PWM automute delay to 20 ms
–	–	–	–	0	1	1	1	Set input automute and PWM automute delay to 30 ms
–	–	–	–	1	0	0	0	Set input automute and PWM automute delay to 40 ms
–	–	–	–	1	0	0	1	Set input automute and PWM automute delay to 50 ms
–	–	–	–	1	0	1	0	Set input automute and PWM automute delay to 60 ms
–	–	–	–	1	0	1	1	Set input automute and PWM automute delay to 70ms
–	–	–	–	1	1	0	0	Set input automute and PWM automute delay to 80 ms
–	–	–	–	1	1	0	1	Set input automute and PWM automute delay to 90 ms
–	–	–	–	1	1	1	0	Set input automute and PWM automute delay to 100 ms
–	–	–	–	1	1	1	1	Set input automute and PWM automute delay to 110 ms
0	0	0	0	–	–	–		Set input automute threshold less than Bit 1 (zero input signal), lowest automute threshold.
0	0	0	1	–	–	–	–	
0	0	1	0	–	–	–	–	Set input automute threshold less than Bit 2
0	0	1	1	–	–	–	–	Set input automute threshold less than Bit 3
0	1	0	0	–	–	–	–	Set input automute threshold less than Bit 4
0	1	0	1	–	–	–	–	Set input automute threshold less than Bit 5
0	1	1	0	–	–	–	–	Set input automute threshold less than Bit 6
0	1	1	1	–	–	–	–	Set input automute threshold less than Bit 7
1	**0**	**0**	**0**	**–**	**–**	**–**	**–**	**Set input automute threshold less than Bit 8**
1	0	0	1	–	–	–	–	Set input automute threshold less than Bit 9
1	0	1	0	–	–	–	–	Set input automute threshold less than Bit 10
1	0	1	1	–	–	–	–	Set input automute threshold less than Bit 11
1	1	0	0	–	–	–	–	Set input automute threshold less than Bit 12
1	1	0	1	–	–	–	–	Set input automute threshold less than Bit 13
1	1	1	0	–	–	–	–	Set input automute threshold less than Bit 14
1	1	1	1	–	–	–	–	Set input automute threshold less than Bit 15

6.11 Automute PWM Threshold and Backend Reset Period (0x15)

Table 6–11. Automute PWM Threshold and Backend Reset Period

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	**0**	**0**	**0**	**–**	**–**	**–**	**–**	**Set PWM automute threshold equals input automute threshold**
0	0	0	1	–	–	–	–	Set PWM automute threshold 1 bit more than input automute threshold
0	0	1	0	–	–	–	–	Set PWM automute threshold 2 bits more than input automute threshold
0	0	1	1	–	–	–	–	Set PWM automute threshold 3 bits more than input automute threshold
0	1	0	0	–	–	–	–	Set PWM automute threshold 4 bits more than input automute threshold
0	1	0	1	–	–	–	–	Set PWM automute threshold 5 bits more than input automute threshold
0	1	1	0	–	–	–	–	Set PWM automute threshold 6 bits more than input automute threshold
0	1	1	1	–	–	–	–	Set PWM automute threshold 7 bits more than input automute threshold
1	0	0	0	–	–	–	–	Set PWM automute threshold equals input automute threshold
1	0	0	1	–	–	–	–	Set PWM automute threshold 1 bit less than input automute threshold
1	0	1	0	–	–	–	–	Set PWM automute threshold 2 bits less than input automute threshold
1	0	1	1	–	–	–	–	Set PWM automute threshold 3 bits less than input automute threshold
1	1	0	0	–	–	–	–	Set PWM automute threshold 4 bits less than input automute threshold
1	1	0	1					Set PWM automute threshold 5 bits less than input automute threshold
1	1	1	0					Set PWM automute threshold 6 bits less than input automute threshold
1	1	1	1					Set PWM automute threshold 7 bits less than input automute threshold
–	–	–	–	0	0	0	0	Set backend reset period < 1 ms
–	–	–	–	0	0	0	1	Set backend reset period 1 ms
–	–	–	–	0	0	1	0	Set backend reset period 2 ms
–	–	–	–	0	0	1	1	Set backend reset period 3 ms
–	–	–	–	0	1	0	0	Set backend reset period 4 ms
–	**–**	**–**	**–**	**0**	**1**	**0**	**1**	**Set backend reset period 5 ms**
–	–	–	–	0	1	1	0	Set backend reset period 6 ms
–	–	–	–	0	1	1	1	Set backend reset period 7 ms
–	–	–	–	1	0	0	0	Set backend reset period 8 ms
–	–	–	–	1	0	0	1	Set backend reset period 9 ms
–	–	–	–	1	0	1	0	Set backend reset period 10 ms
–	–	–	–	1	0	1	1	Set backend reset period 10 ms
–	–	–	–	1	1	X	X	Set backend reset period 10 ms

6.12 Modulation Index Limit Register (0x16)

Table 6–12. Modulation Index Limit Register

D7	D6	D5	D4	D3	D2	D1	D0	LIMIT [DCLKS]	MIN WIDTH [DCLKS]	MODULATION INDEX
					0	0	0	1	2	99.2%
					0	0	1	2	4	98.4%
					0	**1**	**0**	**3**	**6**	**97.7%**
					0	1	1	4	8	96.9%
					1	0	0	5	10	96.1%
					1	0	1	6	12	95.3%
					1	1	0	7	14	94.5%
					1	1	1	8	16	93.8%

6.13 Interchannel Channel Delay Registers (0x1B – 0x22) and Offset Register (0x23)

Channels 1, 2, 3, 4, 5, 6, 7, and 8 are mapped into (0x1B, 0x1C, 0x1D, 0x1E, 0x1F, 0x20, 0x21, and 0x22).

Bits D1 and D0 are *Don't Care*.

Table 6–13. Interchannel Channel Delay Registers

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	**0**	**0**	**0**	**0**	**0**			**Minimum absolute delay, 0 DCLK cycles, default for channel 1**
0	1	1	1	1	1			Maximum positive delay, 31 x 4 DCLK cycles
1	0	0	0	0	0			Maximum negative delay, –32 x 4 DCLK cycles
1	**0**	**0**	**0**	**0**	**0**			**Default value for Channel 1: –32**
0	**0**	**0**	**0**	**0**	**0**			**Default value for Channel 2: 0**
1	**1**	**0**	**0**	**0**	**0**			**Default value for Channel 3: –16**
0	**1**	**0**	**0**	**0**	**0**			**Default value for Channel 4: 16**
1	**0**	**1**	**0**	**0**	**0**			**Default value for Channel 5: –24**
0	**0**	**1**	**0**	**0**	**0**			**Default value for Channel 6: 8**
1	**1**	**1**	**0**	**0**	**0**			**Default value for Channel 7: –8**
0	**1**	**1**	**0**	**0**	**0**			**Default value for Channel 8: 24**

The offset register is mapped into 0x23.

Table 6–14. Channel Offset Register

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Minimum absolute offset, 0 DCLK cycles default for channel 1**
1	1	1	1	1	1	1	1	Maximum absolute delay, 255 DCLK cycles

6.14 Bank Switching Command (0x40)

Bits D31–D24, D22–D19 are *Don't Care*.

Table 6–15. Bank Switching Command

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
								Unused bits

D23	D22	D21	D20	D19	D18	D17	D16	FUNCTION
–					**0**	**0**	**0**	**Manual selection Bank 1**
–					0	0	1	Manual selection Bank 2
–					0	1	0	Manual selection Bank 3
–					0	1	1	Automatic bank selection
–					1	0	0	Update the values in Bank 1
–					1	0	1	Update the values in Bank 2
–					1	1	0	Update the values in Bank 3
0					1	1	1	Update only the bank map
0					x	x	x	Update the bank map using values in D15–D0
1					x	x	x	Do not update the bank map using values in D15–D0

D15	D14	D13	D12	D11	D10	D9	D8	FUNCTION
1	**–**	**–**	**–**	**–**	**–**	**–**	**–**	**32-kHz data rate – Use Bank 1**
–	**1**	**–**	**–**	**–**	**–**	**–**	**–**	**38-kHz data rate – Use Bank 1**
–	**–**	**1**	**–**	**–**	**–**	**–**	**–**	**44.1-kHz data rate – Use Bank 1**
–	**–**	**–**	**1**	**–**	**–**	**–**	**–**	**48-kHz data rate – Use Bank 1**
–	**–**	**–**	**–**	**1**	**–**	**–**	**–**	**88.2-kHz data rate – Use Bank 1**
–	**–**	**–**	**–**	**–**	**1**	**–**	**–**	**96-kHz data rate – Use Bank 1**
–	**–**	**–**	**–**	**–**	**–**	**1**	**–**	**176.4-kHz data rate – Use Bank 1**
–	**–**	**–**	**–**	**–**	**–**	**–**	**1**	**192-kHz data rate – Use Bank 1**
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**Default**

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
1	–	–	–	–	–	–	–	32-kHz data rate – Use Bank 2
–	1	–	–	–	–	–	–	38-kHz data rate – Use Bank 2
–	–	1	–	–	–	–	–	44.1-kHz data rate – Use Bank 2
–	–	–	1	–	–	–	–	48-kHz data rate – Use Bank 2
–	–	–	–	1	–	–	–	88.2-kHz data rate – Use Bank 2
–	–	–	–	–	1	–	–	96-kHz data rate – Use Bank 2
–	–	–	–	–	–	1	–	176.4-kHz data rate – Use Bank 2
–	–	–	–	–	–	–	1	192-kHz data rate – Use Bank 2
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**Default**

6.15 Input Mixer Registers (0x41 – 0x48, Channels 1 – 8)

Input mixers 1, 2, 3, 4, 5, 6, 7, and 8 are mapped into registers 0x41, 0x42, 0x43, 0x44, 0x45, 0x46, 0x47, and 0x48.

Each gain coefficient is in 28-bit (5.23) format so 0x800000 is a gain of 1. Each gain coefficient is written as a 32-bit word with the upper 4 bits not used. For 8-gain coefficients, the total is 32 bytes.

Bold indicates the one channel that is passed through the mixer.

Table 6–16. Input Mixer Registers Format (0x41 – 0x48, Channels 1 – 8)

I^2C SUBADDRESS	TOTAL BYTES	REGISTER FIELDS	DESCRIPTION OF CONTENTS	DEFAULT STATE
0x41	32	**A_to_ipmix[1]**	**SDIN1–Left (Ch 1) A to Input Mixer 1 coefficient (default = 1) U (31:28), A_1 (27:24), A_1 (23:16), A_1 (15:8), A_1 (7:0)**	**0x00, 0x80, 0x00, 0x00**
		B_to_ipmix[1]	SDIN1–Right (Ch 2) B to Input Mixer 1 coefficient (default = 0) U (31:28), B_1 (27:24), B_1 (23:16), B_1 (15:8), B_1 (7:0)	0x00, 0x00, 0x00, 0x00
		C_to_ipmix[1]	SDIN2–Left (Ch 3) C to Input Mixer 1 coefficient (default = 0) U (31:28), C_1 (27:24), C_1 (23:16), C_1 (15:8), C_1 (7:0)	0x00, 0x00, 0x00, 0x00
		D_to_ipmix[1]	SDIN2–Right (Ch 4) D to Input Mixer 1 coefficient (default = 0) U (31:28), D_1 (27:24), D_1 (23:16), D_1 (15:8), D_1 (7:0)	0x00, 0x00, 0x00, 0x00
		E_to_ipmix[1]	SDIN3–Left (Ch 5) E to Input Mixer 1 coefficient (default = 0) U (31:28), E_1 (27:24), E_1 (23:16), E_1 (15:8), E_1 (7:0)	0x00, 0x00, 0x00, 0x00
		F_to_ipmix[1]	SDIN3–Right (Ch 6) F to Input Mixer 1 coefficient (default = 0) U (31:28), F_1 (27:24), F_1 (23:16), F_1 (15:8), F_1 (7:0)	0x00, 0x00, 0x00, 0x00
		G_to_ipmix[1]	SDIN4–Left (Ch 7) G to Input Mixer 1 coefficient (default = 0) U (31:28), G_1 (27:24), G_1 (23:16), G_1 (15:8), G_1 (7:0)	0x00, 0x00, 0x00, 0x00
		H_to_ipmix[1]	SDIN4–Right (Ch 8) H to Input Mixer 1 coefficient (default = 0) U (31:28), H_1 (27:24), H_1 (23:16), H_1 (15:8), H_1 (7:0)	0x00, 0x00, 0x00, 0x00
0x42	32	A_to_ipmix[2]	SDIN1–Left (Ch 1) A to Input Mixer 2 coefficient (default = 0) U (31:28), A_2 (27:24), A_2 (23:16), A_2 (15:8), A_2 (7:0)	0x00, 0x00, 0x00, 0x00
		B_to_ipmix[2]	**SDIN1–Right (Ch 2) B to Input Mixer 2 coefficient (default = 1) U (31:28), B_2 (27:24), B_2 (23:16), B_2 (15:8), B_2 (7:0)**	**0x00, 0x80, 0x00, 0x00**
		C_to_ipmix[2]	SDIN2–Left (Ch 3) C to Input Mixer 2 coefficient (default = 0) U (31:28), C_2(27:24), C_2(23:16), C_2(15:8), C_2(7:0)	0x00, 0x00, 0x00, 0x00
		D_to_ipmix[2]	SDIN2–Right (Ch 4) D to Input Mixer 2 coefficient (default = 0) U (31:28), D_2 (27:24), D_2 (23:16), D_2 (15:8), D_2 (7:0)	0x00, 0x00, 0x00, 0x00
		E_to_ipmix[2]	SDIN3–Left (Ch 5) E to Input Mixer 2 coefficient (default = 0) U (31:28), E_2 (27:24), E_2 (23:16), E_2 (15:8), E_2 (7:0)	0x00, 0x00, 0x00, 0x00
		F_to_ipmix[2]	SDIN3–Right (Ch 6) F to Input Mixer 2 coefficient (default = 0) U (31:28), F_2 (27:24), F_2 (23:16), F_2 (15:8), F_2 (7:0)	0x00, 0x00, 0x00, 0x00
		G_to_ipmix[2]	SDIN4–Left (Ch 7) G to Input Mixer 2 coefficient (default = 0) U (31:28), G_2 (27:24), G_2 (23:16), G_2 (15:8), G_2 (7:0)	0x00, 0x00, 0x00, 0x00
		H_to_ipmix[2]	SDIN4–Right (Ch 8) H to Input Mixer 2 coefficient (default = 0) U (31:28), H_2 (27:24), H_2 (23:16), H_2 (15:8), H_2 (7:0)	0x00, 0x00, 0x00, 0x00

I²C SUBADDRESS	TOTAL BYTES	REGISTER FIELDS	DESCRIPTION OF CONTENTS	DEFAULT STATE
0x43	32	A_to_ipmix[3]	SDIN1–Left (Ch 1) A to Input Mixer 3 coefficient (default = 0) U (31:28), A_3 (27:24), A_3 (23:16), A_3 (15:8), A_3 (7:0)	0x00, 0x00, 0x00, 0x00
		B_to_ipmix[3]	SDIN1–Right (Ch 2) B to Input Mixer 3 coefficient (default = 0) U (31:28), B_3 (27:24), B_3 (23:16), B_3 (15:8), B_3 (7:0)	0x00, 0x00, 0x00, 0x00
		C_to_ipmix[3]	**SDIN2–Left (Ch 3) C to Input Mixer 3 coefficient (default = 1) U (31:28), C_3 (27:24), C_3 (23:16), C_3 (15:8), C_3 (7:0)**	**0x00, 0x80, 0x00, 0x00**
		D_to_ipmix[3]	SDIN2–Right (Ch 4) D to Input Mixer 3 coefficient (default = 0) U (31:28), D_3 (27:24), D_3 (23:16), D_3 (15:8), D_3 (7:0)	0x00, 0x00, 0x00, 0x00
		E_to_ipmix[3]	SDIN3–Left (Ch 5) E to Input Mixer 3 coefficient (default = 0) U (31:28), E_3 (27:24), E_3 (23:16), E_3 (15:8), E_3 (7:0)	0x00, 0x00, 0x00, 0x00
		F_to_ipmix[3]	SDIN3–Right (Ch 6) F to Input Mixer 3 coefficient (default = 0) U (31:28), F_3 (27:24), F_3 (23:16), F_3 (15:8), F_3 (7:0)	0x00, 0x00, 0x00, 0x00
		G_to_ipmix[3]	SDIN4–Left (Ch 7) G to Input Mixer 3 coefficient (default = 0) U (31:28), G_3 (27:24), G_3 (23:16), G_3 (15:8), G_3 (7:0)	0x00, 0x00, 0x00, 0x00
		H_to_ipmix[3]	SDIN4–Right (Ch 8) H to Input Mixer 3 coefficient (default = 0) U (31:28), H_3 (27:24), H_3 (23:16), H_3 (15:8), H_3 (7:0)	0x00, 0x00, 0x00, 0x00
0x44	32	A_to_ipmix[4]	SDIN1–Left (Ch 1) A to Input Mixer 4 coefficient (default = 0) U (31:28), A_4 (27:24), A_4 (23:16), A_4 (15:8), A_4 (7:0)	0x00, 0x00, 0x00, 0x00
		B_to_ipmix[4]	SDIN1–Right (Ch 2) B to Input Mixer 4 coefficient (default = 0) U (31:28), B_4 (27:24), B_4 (23:16), B_4 (15:8), B_4 (7:0)	0x00, 0x00, 0x00, 0x00
		C_to_ipmix[4]	SDIN2–Left (Ch 3) C to Input Mixer 4 coefficient (default = 0) U (31:28), C_4 (27:24), C_4 (23:16), C_4 (15:8), C_4 (7:0)	0x00, 0x00, 0x00, 0x00
		D_to_ipmix[4]	**SDIN2–Right (Ch 4) D to Input Mixer 4 coefficient (default = 1) U (31:28), D_4 (27:24), D_4 (23:16), D_4 (15:8), D_4 (7:0)**	**0x00, 0x80, 0x00, 0x00**
		E_to_ipmix[4]	SDIN3–Left (Ch 5) E to Input Mixer 4 coefficient (default = 0) U (31:28), E_4 (27:24), E_4 (23:16), E_4 (15:8), E_4 (7:0)	0x00, 0x00, 0x00, 0x00
		F_to_ipmix[4]	SDIN3–Right (Ch 6) F to Input Mixer 4 coefficient (default = 0) U (31:28), F_4 (27:24), F_4 (23:16), F_4 (15:8), F_4 (7:0)	0x00, 0x00, 0x00, 0x00
		G_to_ipmix[4]	SDIN4–Left (Ch 7) G to Input Mixer 4 coefficient (default = 0) U (31:28), G_4 (27:24), G_4 (23:16), G_4 (15:8), G_4 (7:0)	0x00, 0x00, 0x00, 0x00
		H_to_ipmix[4]	SDIN4–Right (Ch 8) H to Input Mixer 4 coefficient (default = 0) U (31:28), H_4 (27:24), H_4 (23:16), H_4 (15:8), H_4 (7:0)	0x00, 0x00, 0x00, 0x00
0x45	32	A_to_ipmix[5]	SDIN1–Left (Ch 1) A to Input Mixer 5 coefficient (default = 0) U (31:28), A_5 (27:24), A_5 (23:16), A_5 (15:8), A_5 (7:0)	0x00, 0x00, 0x00, 0x00
		B_to_ipmix[5]	SDIN1–Right (Ch 2) B to Input Mixer 5 coefficient (default = 0) U (31:28), B_5 (27:24), B_5 (23:16), B_5 (15:8), B_5 (7:0)	0x00, 0x00, 0x00, 0x00
		C_to_ipmix[5]	SDIN2–Left (Ch 3) C to Input Mixer 5 coefficient (default = 0) U (31:28), C_5 (27:24), C_5 (23:16), C_5 (15:8), C_5 (7:0)	0x00, 0x00, 0x00, 0x00
		D_to_ipmix[5]	SDIN2–Right (Ch 4) D to Input Mixer 5 coefficient (default = 0) U (31:28), D_5 (27:24), D_5 (23:16), D_5 (15:8), D_5 (7:0)	0x00, 0x00, 0x00, 0x00
		E_to_ipmix[5]	**SDIN3–Left (Ch 5) E to Input Mixer 5 coefficient (default = 1) U (31:28), E_5 (27:24), E_5 (23:16), E_5 (15:8), E_5 (7:0)**	**0x00, 0x80, 0x00, 0x00**
		F_to_ipmix[5]	SDIN3–Right (Ch 6) F to Input Mixer 5 coefficient (default = 0) U (31:28), F_5 (27:24), F_5 (23:16), F_5 (15:8), F_5 (7:0)	0x00, 0x00, 0x00, 0x00
		G_to_ipmix[5]	SDIN4–Left (Ch 7) G to Input Mixer 5 coefficient (default = 0) U (31:28), G_5 (27:24), G_5 (23:16), G_5 (15:8), G_5 (7:0)	0x00, 0x00, 0x00, 0x00
		H_to_ipmix[5]	SDIN4–Right (Ch 8) H to Input Mixer 5 coefficient (default = 0) U (31:28), H_5 (27:24), H_5 (23:16), H_5 (15:8), H_5 (7:0)	0x00, 0x00, 0x00, 0x00

I²C SUBADDRESS	TOTAL BYTES	REGISTER FIELDS	DESCRIPTION OF CONTENTS	DEFAULT STATE
0x46	32	A_to_ipmix[6]	SDIN1–Left (Ch 1) A to Input Mixer 6 coefficient (default = 0) U (31:28), A_6 (27:24), A_6 (23:16), A_6 (15:8), A_6 (7:0)	0x00, 0x00, 0x00, 0x00
		B_to_ipmix[6]	SDIN1–Right (Ch 2) B to Input Mixer 6 coefficient (default = 0) U (31:28), B_6 (27:24), B_6 (23:16), B_6 (15:8), B_6 (7:0)	0x00, 0x00, 0x00, 0x00
		C_to_ipmix[6]	SDIN2–Left (Ch 3) C to Input Mixer 6 coefficient (default = 0) U (31:28), C_6 (27:24), C_6 (23:16), C_6 (15:8), C_6 (7:0)	0x00, 0x00, 0x00, 0x00
		D_to_ipmix[6]	SDIN2–Right (Ch 4) D to Input Mixer 6 coefficient (default = 0) U (31:28), D_6 (27:24), D_6 (23:16), D_6 (15:8), D_6 (7:0)	0x00, 0x00, 0x00, 0x00
		E_to_ipmix[6]	SDIN3–Left (Ch 5) E to Input Mixer 6 coefficient (default = 0) U (31:28), E_6 (27:24), E_6 (23:16), E_6 (15:8), E_6 (7:0)	0x00, 0x00, 0x00, 0x00
		F_to_ipmix[6]	**SDIN3–Right (Ch 6) F to Input Mixer 6 coefficient (default = 1) U (31:28), F_6 (27:24), F_6 (23:16), F_6 (15:8), F_6 (7:0)**	**0x00, 0x80, 0x00, 0x00**
		G_to_ipmix[6]	SDIN4–Left (Ch 7) G to Input Mixer 6 coefficient (default = 0) U (31:28), G_6 (27:24), G_6 (23:16), G_6 (15:8), G_6 (7:0)	0x00, 0x00, 0x00, 0x00
		H_to_ipmix[6]	SDIN4–Right (Ch 8) H to Input Mixer 6 coefficient (default = 0) U (31:28), H_6 (27:24), H_6 (23:16), H_6 (15:8), H_6 (7:0)	0x00, 0x00, 0x00, 0x00
0x47	32	A_to_ipmix[7]	SDIN1–Left (Ch 1) A to Input Mixer 7 coefficient (default = 0) U (31:28), A_7 (27:24), A_7 (23:16), A_7 (15:8), A_7 (7:0)	0x00, 0x00, 0x00, 0x00
		B_to_ipmix[7]	SDIN1–Right (Ch 2) B to Input Mixer 7 coefficient (default = 0) U (31:28), B_7 (27:24), B_7 (23:16), B_7 (15:8), B_7 (7:0)	0x00, 0x00, 0x00, 0x00
		C_to_ipmix[7]	SDIN2–Left (Ch 3) C to Input Mixer 7 coefficient (default = 0) U (31:28), C_7 (27:24), C_7 (23:16), C_7 (15:8), C_7 (7:0)	0x00, 0x00, 0x00, 0x00
		D_to_ipmix[7]	SDIN2–Right (Ch 4) D to Input Mixer 7 coefficient (default = 0) U (31:28), D_7 (27:24), D_7 (23:16), D_7 (15:8), D_7 (7:0)	0x00, 0x00, 0x00, 0x00
		E_to_ipmix[7]	SDIN3–Left (Ch 5) E to Input Mixer 7 coefficient (default = 0) U (31:28), E_7 (27:24), E_7 (23:16), E_7 (15:8), E_7 (7:0)	0x00, 0x00, 0x00, 0x00
		F_to_ipmix[7]	SDIN3–Right (Ch 6) F to Input Mixer 7 coefficient (default = 0) U (31:28), F_7 (27:24), F_7 (23:16), F_7 (15:8), F_7 (7:0)	0x00, 0x00, 0x00, 0x00
		G_to_ipmix[7]	**SDIN4–Left (Ch 7) G to Input Mixer 7 coefficient (default = 1) U (31:28), G_7 (27:24), G_7 (23:16), G_7 (15:8), G_7 (7:0)**	**0x00, 0x80, 0x00, 0x00**
		H_to_ipmix[7]	SDIN4–Right (Ch 8) H to Input Mixer 7 coefficient (default = 0) U (31:28), H_7 (27:24), H_7 (23:16), H_7 (15:8), H_7 (7:0)	0x00, 0x00, 0x00, 0x00
0x48	32	A_to_ipmix[8]	SDIN1–Left (Ch 1) A to Input Mixer 8 coefficient (default = 0) U (31:28), A_8 (27:24), A_8 (23:16), A_8 (15:8), A_8 (7:0)	0x00, 0x00, 0x00, 0x00
		B_to_ipmix[8]	SDIN1–Right (Ch 2) B to Input Mixer 8 coefficient (default = 0) U (31:28), B_8 (27:24), B_8 (23:16), B_8 (15:8), B_8 (7:0)	0x00, 0x00, 0x00, 0x00
		C_to_ipmix[8]	SDIN2–Left (Ch 3) C to Input Mixer 8 coefficient (default = 0) U (31:28), C_8 (27:24), C_8 (23:16), C_8 (15:8), C_8 (7:0)	0x00, 0x00, 0x00, 0x00
		D_to_ipmix[8]	SDIN2–Right (Ch 4) D to Input Mixer 8 coefficient (default = 0) U (31:28), D_8 (27:24), D_8 (23:16), D_8 (15:8), D_8 (7:0)	0x00, 0x00, 0x00, 0x00
		E_to_ipmix[8]	SDIN3–Left (Ch 5) E to Input Mixer 8 coefficient (default = 0) U (31:28), E_8 (27:24), E_8 (23:16), E_8 (15:8), E_8 (7:0)	0x00, 0x00, 0x00, 0x00
		F_to_ipmix[8]	SDIN3–Right (Ch 6) F to Input Mixer 8 coefficient (default = 0) U (31:28), F_8 (27:24), F_8 (23:16), F_8 (15:8), F_8 (7:0)	0x00, 0x00, 0x00, 0x00
		G_to_ipmix[8]	SDIN4–Left (Ch 7) G to Input Mixer 8 coefficient (default = 0) U (31:28), G_8 (27:24), G_8 (23:16), G_8 (15:8), G_8 (7:0)	0x00, 0x00, 0x00, 0x00
		H_to_ipmix[8]	**SDIN4–Right (Ch 8) H to Input Mixer 8 coefficient (default = 1) U (31:28), H_8 (27:24), H_8 (23:16), H_8 (15:8), H_8 (7:0)**	**0x00, 0x80, 0x00, 0x00**

6.16 Bass Management Registers (0x49 – 0x50)

Registers 0x49 – 0x50 provide configuration control for bass mangement.

Each gain coefficient is in 28-bit (5.23) format so 0x800000 is a gain of 1. Each gain coefficient is written as a 32-bit word with the upper four bits not used.

Table 6–17. Bass Management Registers Format (0x49 – 0x50)

SUBADDRESS	TOTAL BYTES	REGISTER NAME	DESCRIPTION OF CONTENTS	DEFAULT STATE
0x49	4	ipmix_1_to_ch8	Input Mixer 1 to Ch 8 Mixer coefficient (default = 0) U (31:28), ipmix18 (27:24), ipmix18 (23:16), ipmix18 (15:8), ipmix18 (7:0)	0x00, 0x00, 0x00, 0x00
0x4A	4	ipmix_2_to_ch8	Input Mixer 1 to Ch 8 Mixer coefficient (default = 0) U (31:28), ipmix28 (27:24), ipmix28 (23:16), ipmix28 (15:8), ipmix28 (7:0)	0x00, 0x00, 0x00, 0x00
0x4B	4	ipmix_7_to_ch12	Input Mixer 7 to Ch 1 and Ch 2 Mixer coefficient (default = 0) U (31:28), ipmix72 (27:24), ipmix72 (23:16), ipmix72 (15:8), ipmix72 (7:0)	0x00, 0x00, 0x00, 0x00
0x4C	4	Ch7_bp_bq2	Ch 7 Biquad-2 By-pass coefficient (default = 0) U (31:28), ch7_bp_bq2 (27:24), ch7_bp_bq2 (23:16), ch7_bp_bq2 (15:8), ch7_bp_bq2 (7:0)	0x00, 0x00, 0x00, 0x00
0x4D	4	Ch7_bq2	Ch 7 Biquad-2 Inline coefficient (default = 1) U (31:28), ch6_bq2 (27:24), ch6_bq2 (23:16), ch6_bq2 (15:8), ch6_bq2 (7:0)	0x00, 0x80, 0x00, 0x00
0x4E	4	ipmix_8_to_ch12	Ch 8 Biquad-2 Output to Ch1 Mixer and Ch2 Mixer coefficient (default = 0) U (31:28), ipmix8_12 (27:24), ipmix8_12 (23:16), ipmix8_12 (15:8), ipmix8_12 (7:0)	0x00, 0x00, 0x00, 0x00
0x4F	4	Ch8_bp_bq2	Ch 8 Biquad-2 By-pass coefficient (default = 0) 0U (31:28), ch8_bp_bq2 (27:24), ch8_bp_bq2 (23:16), ch8_bp_bq2 (15:8), ch8_bp_bq2 (7:0)	0x00, 0x00, 0x00, 0x00
0x50	4	Ch8_bq2	Ch 8 Biquad-2 Inline coefficient (default = 1) U (31:28), ch7_bq2 (27:24), ch7_bq2 (23:16), ch7_bq2 (15:8), ch7_bq2 (7:0)	0x00, 0x80, 0x00, 0x00

6.17 Biquad Filters Register (0x51 – 0x88)

Table 6–18. Biquad Filters Registers Format (0x51 – 0x88)

I^2C SUBADDRESS	TOTAL BYTES	REGISTER NAME	DESCRIPTION OF CONTENTS	DEFAULT STATE
0x51 – 0x57	20/Reg.	Ch1_bq[1] – [7]	Ch 1 Biquads 1 – 7. See Table 6–19 for bit definition.	See Table 6–19
0x58 – 0x5E	20/Reg.	Ch2_bq[1] – [7]	Ch 2 Biquads 1 – 7. See Table 6–19 for bit definition.	See Table 6–19
0x5F – 0x65	20/Reg.	Ch3_bq[1] – [7]	Ch 3 Biquads 1 – 7. See Table 6–19 for bit definition.	See Table 6–19
0x66 – 0x6C	20/Reg.	Ch4_bq[1] – [7]	Ch 4 Biquads 1 – 7. See Table 6–19 for bit definition.	See Table 6–19
0x6D – 0x73	20/Reg.	Ch5_bq[1] – [7]	Ch 5 Biquads 1 – 7. See Table 6–19 for bit definition.	See Table 6–19
0x74 – 0x7A	20/Reg.	Ch6_bq[1] – [7]	Ch 6 Biquads 1 – 7. See Table 6–19 for bit definition.	See Table 6–19
0x7B – 0x81	20/Reg.	Ch7_bq[1] – [7]	Ch 7 Biquads 1 – 7. See Table 6–19 for bit definition.	See Table 6–19
0x82 – 0x88	20/Reg.	Ch8_bq[1] – [7]	Ch 8 Biquads 1 – 7. See Table 6–19 for bit definition.	See Table 6–19

Each gain coefficient is in 28-bit (5.23) format so 0x800000 is a gain of 1. Each gain coefficient is written as a 32-bit word with the upper four bits not used.

Table 6–19. Contents of One 20-Byte Biquad Filter Register Format (Default = All-pass)

DESCRIPTION	REGISTER FIELD CONTENTS	DEFAULT GAIN COEFFICIENT VALUES	
		DECIMAL	HEX
b_0 Coefficient	U (31:28), b0 (27:24), b0 (23:16), b0 (15:8), b0 (7:0)	**1.0**	0x00, **0x80**, 0x00, 0x00
b_1 Coefficient	U (31:28), b1 (27:24), b1 (23:16), b1 (15:8), b1 (7:0)	0.0	0x00, 0x00, 0x00, 0x00
b_2 Coefficient	U (31:28), b2 (27:24), b2 (23:16), b2 (15:8), b2 (7:0)	0.0	0x00, 0x00, 0x00, 0x00
a_1 Coefficient	U (31:28), a1 (27:24), a1 (23:16), a1 (15:8), a1 (7:0)	0.0	0x00, 0x00, 0x00, 0x00
a_2 Coefficient	U (31:28), a2 (27:24), a2 (23:16), a2 (15:8), a2 (7:0)	0.0	0x00, 0x00, 0x00, 0x00

6.18 Bass and Treble Bypass Register (0x89 – 0x90, Channels 1 – 8)

Channels 1, 2, 3, 4, 5, 6, 7, and 8 are mapped into registers 0x89, 0x8A, 0x8B, 0x8C,0x8D, 0x8E, 0x8F, and 0x90. Eight bytes are written for each channel. Each gain coefficient is in 28-bit (5.23) format so 0x800000 is a gain of 1. Each gain coefficient is written as a 32-bit word with the upper four bits not used.

Table 6–20. Bass and Treble Bypass Register Format (0x89–0x90)

REGISTER NAME	TOTAL BYTES	CONTENTS	INITIALIZATION VALUE
Channel bass and treble bypass	8	U 31:28), Bypass (27:24), Bypass (23:16), Bypass (15:8), Bypass (7:0)	0x00, 0x80, 0x00, 0x00
Channel bass and treble inline		U (31:28), Inline (27:24), Inline (23:16), Inline (15:8), Inline (7:0)	0x00, 0x00, 0x00, 0x00

6.19 Loudness Registers (0x91 – 0x95)

Table 6–21. Loudness Registers Format (0x91 – 0x95)

I^2C SUBADDRESS	TOTAL BYTES	REGISTER NAME	DESCRIPTION OF CONTENTS	DEFAULT STATE
0x91	4	Loudness Log2 Gain (LG)	U (31:28), LG (27:24), LG (23:16), LG (15:8), LG (7:0)	0xFF, 0xC0, 0x00, 0x00
0x92	8	Loudness Log2 Offset (LO)	U (31:24), U (23:16), LO (15:8), LO (7:0)	0x00, 0x00, 0x00, 0x00,
		Loudness Log2 LO	LO (31:24), LO (23:16), LO (15:8), LO (7:0)	0x00, 0x00, 0x00, 0x00,
0x93	4	Loudness Gain (G)	U (31:28), G (27:24), G (23:16), G (15:8), G (7:0)	0x00, 0x00, 0x00, 0x00,
0x94	8	Loudness Offset Upper 16 bits (O)	U (31:24), U (23:16), O (15:8), O (7:0)	0x00, 0x00, 0x00, 0x00,
		Loudness O Offset Lower 32 bits (O)	O (31:24), O (23:16), O (15:8), O (7:0)	0x00, 0x00, 0x00, 0x00,
0x95	20	Loudness Biquad (b0)	U (31:28), b0 (27:24), b0 (23:16), b0 (15:8), b0 (7:0)	0x00, 0x00, 0xD5, 0x13,
		Loudness Biquad (b1)	U (31:28), b1 (27:24), b1 (23:16), b1 (15:8), b1 (7:0)	0x00, 0x00, 0x00, 0x00,
		Loudness Biquad (b2)	U (31:28), b2 (27:24), b2 (23:16), b2 (15:8), b2 (7:0)	0x0F, 0xFF, 0x2A, 0xED,
		Loudness Biquad (a1)	U (31:28), a1 (27:24), a1 (23:16), a1 (15:8), a1 (7:0)	0x00, 0xFE, 0x50, 0x45,
		Loudness Biquad (a2)	U (31:28), a2 (27:24), a2 (23:16), a2 (15:8), a2 (7:0)	0x0F, 0x81, 0xAA, 0x27

6.20 DRC1 Control (0x96, Channels 1–7)

Bits D31 – D14 are *Don't Care*.

Table 6–22. DCR1 Control (0x96, Channels 1–7)

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
								Unused bits

D23	D22	D21	D20	D19	D18	D17	D16	FUNCTION
								Unused bits

D15	D14	D13	D12	D11	D10	D9	D8	FUNCTION
		0	**0**	**–**	**–**	**–**	**–**	**Channel 1 (node j): No DRC**
		0	1	–	–	–	–	Channel 1 (node j): Pre-volume DRC
		1	0	–	–	–	–	Channel 1 (node j): Post-volume DRC
		1	1	–	–	–	–	Channel 1 (node j): No DRC
		–	**–**	**0**	**0**	**–**	**–**	**Channel 2 (node l): No DRC**
		–	–	0	1	–	–	Channel 2 (node l): Pre-volume DRC
		–	–	1	0	–	–	Channel 2 (node l): Post-volume DRC
		–	–	1	1	–	–	Channel 2 (node i): No DRC
		–	**–**	**–**	**–**	**0**	**0**	**Channel 3 (node m): No DRC**
		–	–	–	–	0	1	Channel 3 (node m): Pre-volume DRC
		–	–	–	–	1	0	Channel 3 (node m): Post-volume DRC
		–	–	–	–	1	1	Channel 3 (node m): No DRC

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	**0**	**–**	**–**	**–**	**–**	**–**	**–**	**Channel 4 (node n): No DRC**
0	1	–	–	–	–	–	–	Channel 4 (node n): Pre-volume DRC
1	0	–	–	–	–	–	–	Channel 4 (node n): Post-volume DRC
1	1	–	–	–	–	–	–	Channel 4 (node n): No DRC
–	**–**	**0**	**0**	**–**	**–**	**–**	**–**	**Channel 5 (node o): No DRC**
–	–	0	1	–	–	–	–	Channel 5 (node o): Pre-volume DRC
–	–	1	0	–	–	–	–	Channel 5 (node o): Post-volume DRC
–	–	1	1	–	–	–	–	Channel 5 (node o): No DRC
–	**–**	**–**	**–**	**0**	**0**	**–**	**–**	**Channel 6 (node p): No DRC**
–	–	–	–	0	1	–	–	Channel 6 (node p): Pre-volume DRC
–	–	–	–	1	0	–	–	Channel 6 (node p): Post-volume DRC
–	–	–	–	1	1	–	–	Channel 6 (node p): No DRC
–	**–**	**–**	**–**	**–**	**–**	**0**	**0**	**Channel 7 (node q): No DRC**
–	–	–	–	–	–	0	1	Channel 7 (node q): Pre-volume DRC
–	–	–	–	–	–	1	0	Channel 7 (node q): Post-volume DRC
–	–	–	–	–	–	1	1	Channel 7 (node q): No DRC

6.21 DRC2 Control (0x97, Channel 8)

Table 6–23. DRC2 Control (0x97, Channel 8)

D31 – D2		D1	D0	FUNCTION
0	**0**	**0**	**0**	**Channel 8 (node r): No DRC**
0	0	0	1	Channel 8 (node r): Pre-volume DRC
0	0	1	0	Channel 8 (node r): Post-volume DRC
0	0	1	1	Channel 8 (node r): No DRC

6.22 DRC1 Data Registers (0x98 – 0x9C)

DRC1 applies to channels 1, 2, 3, 4, 5, 6, and 7.

Table 6–24. DRC1 Data Registers

I²C SUBADDRESS	TOTAL BYTES	REGISTER NAME	DESCRIPTION OF CONTENTS	DEFAULT STATE
0x98	8	Channel 1, 2, 3, 4, 5, 6, and 7 DRC1 Energy	U (31:28), E (27:24), E (23:16), E (15:8), E (7:0)	0x00, 0x00, 0x88, 0x3F
		Channel 1, 2, 3, 4, 5, 6, and 7 DRC1 (1– Energy)	U (31:28), 1–E (27:24), 1–E (23:16), 1–E (15:8), 1–E (7:0)	0x00, 0x7F, 0x77, 0xC0
0x99	16	Channel 1, 2, 3, 4, 5, 6, and 7 DRC1 Threshold Upper 16 bits (T1)	U (31:24), U (23:16), T1 (15:8), T1 (7:0)	0x00, 0x00, 0x00, 0x00
		Channel 1, 2, 3, 4, 5, 6, and 7 DRC1 Threshold Lower 32 bits (T1)	T1 (31:24), T1 (23:16), T1 (15:8), T1 (7:0)	0x0B, 0x20, 0xE2, 0xB2
		Channel 1, 2, 3, 4, 5, 6, and 7 DRC1 Threshold Upper 16 bits (T2)	U (31:24), U (23:16), T2 (15:8), T2 (7:0)	0x00, 0x00, 0x00, 0x00
		Channel 1, 2, 3, 4, 5, 6, and 7 DRC1 Threshold Lower 32 bits (T2)	T2 (31:24), T2 (23:16), T2 (15:8), T2 (7:0)	0x06, 0xF9, 0xDE, 0x58
0x9A	12	Channel 1, 2, 3, 4, 5, 6, and 7 DRC1 slope (k0)	U (31:28), k0 (27:24), k0 (23:16), k0 (15:8), k0 (7:0)	0x00, 0x40, 0x00, 0x00
		Channel 1, 2, 3, 4, 5, 6, and 7 DRC1 slope (k1)	U (31:28), k1 (27:24), k1 (23:16), k1 (15:8), k1 (7:0)	0x0F, 0xC0, 0x00, 0x00
		Channel 1, 2, 3, 4, 5, 6, and 7 DRC1 slope (k2)	U (31:28), k2 (27:24), k2 (23:16), k2 (15:8), k2 (7:0)	0x0F, 0x90, 0x00, 0x00
0x9B	16	Channel 1, 2, 3, 4, 5, 6, and 7 DRC1 Offset 1 Upper 16 bits (O1)	U (31:24), U (23:16), O1 (15:8), O1 (7:0)	0x00, 0x00, 0xFF, 0xFF
		Channel 1, 2, 3, 4, 5, 6, and 7 DRC1 Offset 1 Lower 32 bits (O1)	O1 (31:24), O1 (23:16), O1 (15:8), O1 (7:0)	0xFF, 0x82, 0x30, 0x98
		Channel 1, 2, 3, 4, 5, 6, and 7 DRC1 Offset 2 Upper 16 bits (O2)	U (31:24), U (23:16), O2 (15:8), O2 (7:0)	0x00, 0x00, 0x00, 0x00
		Channel 1, 2, 3, 4, 5, 6, and 7 DRC1 Offset 2 Lower 32 bits (O2)	O2 (31:24), O2 (23:16), O2 (15:8), O2 (7:0)	0x01, 0x95, 0xB2, 0xC0
0x9C	16	Channel 1, 2, 3, 4, 5, 6, and 7 DRC1 Attack	U (31:28), A (27:24), A (23:16), A (15:8), A (7:0)	0x00, 0x00, 0x88, 0x3F
		Channel 1, 2, 3, 4, 5, 6, and 7 DRC1 (1– Attack)	U (31:28), 1–A (27:24), 1–A (23:16), 1–A (15:8), 1–A (7:0)	0x00, 0x7F, 0x77, 0xC0
		Channel 1, 2, 3, 4, 5, 6, and 7 DRC1 Decay	U (31:28), D (27:24), D (23:16), D (15:8), D (7:0)	0x00, 0x00, 0x00, 0xAE
		Channel 1, 2, 3, 4, 5, 6, and 7 DRC1 (1– Decay)	U (31:28), 1–D (27:24), 1–D (23:16), 1–D (15:8), 1–D (7:0)	0x00, 0x7F, 0xFF, 0x51

6.23 DRC2 Data Registers (0x9D – 0xA1)

DRC2 applies to channel 8.

Table 6–25. DRC2 Data Registers

I²C SUBADDRESS	TOTAL BYTES	REGISTER NAME	DESCRIPTION OF CONTENTS	DEFAULT STATE
0x9D	8	Channel 8 DRC2 Energy	U (31:28), E (27:24), E (23:16), E (15:8), E (7:0)	0x00, 0x00, 0x88, 0x3F
		Channel 8 DRC2 (1– Energy)	U (31:28), 1–E (27:24), 1–E (23:16), 1–E (15:8), 1–E (7:0)	0x00, 0x7F, 0x77, 0xC0
0x9E	16	Channel 8 DRC2 Threshold Upper 16 bits (T1)	U (31:24), U (23:16), T1 (15:8), T1 (7:0)	0x00, 0x00, 0x00, 0x00
		Channel 8 DRC2 Threshold Lower 32 bits (T1)	T1 (31:24), T1 (23:16), T1 (15:8), T1 (7:0)	0x0B, 0x20, 0xE2, 0xB2
		Channel 8 DRC2 Threshold Upper 16 bits (T2)	U (31:24), U (23:16), T2 (15:8), T2 (7:0)	0x00, 0x00, 0x00, 0x00
		Channel 8 DRC2 Threshold Lower 32 bits (T2)	T2 (31:24), T2 (23:16), T2 (15:8), T2 (7:0)	0x06, 0xF9, 0xDE, 0x58
0x9F	12	Channel 8 DRC2 slope (k0)	U (31:28), k0 (27:24), k0 (23:16), k0 (15:8), k0 (7:0)	0x00, 0x40, 0x00, 0x00
		Channel 8 DRC2 slope (k1)	U (31:28), k1 (27:24), k1 (23:16), k1 (15:8), k1 (7:0)	0x0F, 0xC0, 0x00, 0x00
		Channel 8 DRC2 slope (k2)	U (31:28), k2 (27:24), k2 (23:16), k2 (15:8), k2 (7:0)	0x0F, 0x90, 0x00, 0x00
0xA0	16	Channel 8 DRC2 Offset 1 Upper 16 bits (O1)	U (31:24), U (23:16), O1 (15:8), O1 (7:0)	0x00, 0x00, 0xFF, 0xFF,
		Channel 8 DRC2 Offset 1 Lower 32 bits (O1)	O1 (31:24), O1 (23:16), O1 (15:8), O1 (7:0)	0xFF, 0x82, 0x30, 0x98
		Channel 8 DRC2 Offset 2 Upper 16 bits (O2)	U (31:24), U (23:16), O2 (15:8), O2 (7:0)	0x00, 0x00, 0x00, 0x00
		Channel 8 DRC2 Offset 2 Lower 32 bits (O2)	O2 (31:24), O2 (23:16), O2 (15:8), O2 (7:0)	0x01, 0x95, 0xB2, 0xC0
0xA1	16	Channel 8 DRC2 Attack	U (31:28), A (27:24), A (23:16), A (15:8), A (7:0)	0x00, 0x00, 0x88, 0x3F
		Channel 8 DRC2 (1– Attack)	U (31:28), 1–A (27:24), 1–A (23:16), 1–A (15:8), 1–A (7:0)	0x00, 0x7F, 0x77, 0xC0
		Channel 8 DRC2 Decay	U (31:28), D (27:24), D (23:16), D (15:8), D (7:0)	0x00, 0x00, 0x00, 0xAE
		Channel 8 DRC2 (1– Decay)	U (31:28), 1–D (27:24), 1–D (23:16), 1–D (15:8), 1–D (7:0)	0x00, 0x7F, 0xFF, 0x51

6.24 DRC Bypass Registers (0xA2 – 0xA9)

DRC bypass/inline for channels 1, 2, 3, 4, 5, 6, 7, and 8 are mapped into registers 0xA2, 0xA3, 0xA4, 0xA5,0xA6, 0xA7, 0xA8, and 0xA9. 8−bytes are written for each channel. Each gain coefficient is in 28-bit (5.23) format so 0x00800000 is a gain of 1. Each gain coefficient is written as a 32-bit word with the upper 4 bits not used.

To enable DRC for a given channel (with unity gain), bypass = 0x00000000 and inline = 0x00800000.

To disable DRC for a given channel, bypass = 0x00800000 and inline = 0x00000000.

Table 6−26. DRC Bypass Registers Format (0xA2−0xA9)

REGISTER NAME	TOTAL BYTES	CONTENTS	INITIALIZATION VALUE
Channel bass DRC bypass	8	U (31:28), bypass (27:24), bypass (23:16), bypass (15:8), bypass (7:0)	0x00, 0x80, 0x00, 0x00
Channel DRC inline		U (31:28), inline (27:24), inline (23:16), inline (15:8), inline (7:0)	0x00, 0x00, 0x00, 0x00

6.25 8x2 Output Mixer Registers (0xAA – 0xAF)

Output mixers for channels 1−6 map to registers 0xAA − 0xAF.

Total data per register is 8 bytes.

Table 6−27. Output Mixer Control Register Format (Upper 4 Bytes)

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	0	0	0					Select channel 1 to output mixer
0	0	0	1					Select channel 2 to output mixer
0	0	1	0					Select channel 3 to output mixer
0	0	1	1					Select channel 4 to output mixer
0	1	0	0					Select channel 5 to output mixer
0	1	0	1					Select channel 6 to output mixer
0	1	1	0					Select channel 7 to output mixer
0	1	1	1					Select channel 8 to output mixer
				G27	G26	G25	G24	Selected channel gain (upper 4 bits)

D23	D22	D21	D20	D19	D18	D17	D16	FUNCTION
G23	G22	G21	G20	G19	G18	G17	G16	Selected channel gain (continued)

D15	D14	D13	D12	D11	D10	D9	D8	FUNCTION
G15	G14	G13	G12	G11	G10	G9	G8	Selected channel gain (continued)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
G7	G6	G5	G4	G3	G2	G1	G0	Selected channel gain (lower 8 bits)

Table 6–28. Output Mixer Control (Lower 4 Bytes)

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	0	0	0					Select channel 1 to output mixer
0	0	0	1					Select channel 2 to output mixer
0	0	1	0					Select channel 3 to output mixer
0	0	1	1					Select channel 4 to output mixer
0	1	0	0					Select channel 5 to output mixer
0	1	0	1					Select channel 6 to output mixer
0	1	1	0					Select channel 7 to output mixer
0	1	1	1					Select channel 8 to output mixer
				G27	G26	G25	G24	Selected channel gain (upper 4 bits)

D23	D22	D21	D20	D19	D18	D17	D16	FUNCTION
G23	G22	G21	G20	G19	G18	G17	G16	Selected channel gain (continued)

D15	D14	D13	D12	D11	D10	D9	D8	FUNCTION
G15	G14	G13	G12	G11	G10	G9	G8	Selected channel gain (continued)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
G7	G6	G5	G4	G3	G2	G1	G0	Selected channel gain (lower 8 bits)

6.26 8x3 Output Mixer Registers (0xB0 – 0xB1)

Output mixers for channels 7 and 8 map to registers 0xB0 and 0xB1.

Total data per register is 12 bytes.

Table 6–29. Output Mixer Control (Upper 4 Bytes)

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	0	0	0					Select channel 1 to output mixer
0	0	0	1					Select channel 2 to output mixer
0	0	1	0					Select channel 3 to output mixer
0	0	1	1					Select channel 4 to output mixer
0	1	0	0					Select channel 5 to output mixer
0	1	0	1					Select channel 6 to output mixer
0	1	1	0					Select channel 7 to output mixer
0	1	1	1					Select channel 8 to output mixer
				G27	G26	G25	G24	Selected channel gain (upper 4 bits)

D23	D22	D21	D20	D19	D18	D17	D16	FUNCTION
G23	G22	G21	G20	G19	G18	G17	G16	Selected channel gain (continued)

D15	D14	D13	D12	D11	D10	D9	D8	FUNCTION
G15	G14	G13	G12	G11	G10	G9	G8	Selected channel gain (continued)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
G7	G6	G5	G4	G3	G2	G1	G0	Selected channel gain (lower 8 bits)

Table 6–30. Output Mixer Control (Middle 4 Bytes)

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	0	0	0					Select channel 1 to output mixer
0	0	0	1					Select channel 2 to output mixer
0	0	1	0					Select channel 3 to output mixer
0	0	1	1					Select channel 4 to output mixer
0	1	0	0					Select channel 5 to output mixer
0	1	0	1					Select channel 6 to output mixer
0	1	1	0					Select channel 7 to output mixer
0	1	1	1					Select channel 8 to output mixer
				G27	G26	G25	G24	Selected channel gain (upper 4 bits)

D23	D22	D21	D20	D19	D18	D17	D16	FUNCTION
G23	G22	G21	G20	G19	G18	G17	G16	Selected channel gain (continued)

D15	D14	D13	D12	D11	D10	D9	D8	FUNCTION
G15	G14	G13	G12	G11	G10	G9	G8	Selected channel gain (continued)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
G7	G6	G5	G4	G3	G2	G1	G0	Selected channel gain (lower 8 bits)

Table 6–31. Output Mixer Control (Lower 4 Bytes)

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	0	0	0					Select channel 1 to output mixer
0	0	0	1					Select channel 2 to output mixer
0	0	1	0					Select channel 3 to output mixer
0	0	1	1					Select channel 4 to output mixer
0	1	0	0					Select channel 5 to output mixer
0	1	0	1					Select channel 6 to output mixer
0	1	1	0					Select channel 7 to output mixer
0	1	1	1					Select channel 8 to output mixer
				G27	G26	G25	G24	Selected channel gain (upper 4 bits)

D23	D22	D21	D20	D19	D18	D17	D16	FUNCTION
G23	G22	G21	G20	G19	G18	G17	G16	Selected channel gain (continued)

D15	D14	D13	D12	D11	D10	D9	D8	FUNCTION
G15	G14	G13	G12	G11	G10	G9	G8	Selected channel gain (continued)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
G7	G6	G5	G4	G3	G2	G1	G0	Selected channel gain (lower 8 bits)

6.27 Volume Biquad Register (0xCF)

Each gain coefficient is in 28-bit (5.23) format so 0x800000 is a gain of 1. Each gain coefficient is written as a 32-bit word with the upper four bits not used.

Table 6–32. Volume Biquad Register Format (Default = All-pass)

DESCRIPTION	REGISTER FIELD CONTENTS	DEFAULT GAIN COEFFICIENT VALUES	
		DECIMAL	HEX
b_o Coefficient	0U (31:28), b0 (27:24), b0 (23:16), b0 (15:8), b0 (7:0)	**1.0**	0x00, **0x80**, 0x00, 0x00
b_1 Coefficient	U (31:28), b1 (27:24), b1 (23:16), b1 (15:8), b1 (7:0)	0.0	0x00, 0x00, 0x00, 0x00
b_2 Coefficient	U (31:28), b2 (27:24), b2 (23:16), b2 (15:8), b2 (7:0)	0.0	0x00, 0x00, 0x00, 0x00
a_1 Coefficient	0U (31:28), a1 (27:24), a1 (23:16), a1 (15:8), a1 (7:0)	0.0	0x00, 0x00, 0x00, 0x00
a_2 Coefficient	U (31:28), a2 (27:24), a2 (23:16), a2 (15:8), a2 (7:0)	0.0	0x00, 0x00, 0x00, 0x00

6.28 Volume Treble and Bass Slew Rates (0xD0)

Table 6–33. Volume Gain Update Rate (Slew Rate)

D31–D10	D9	D8	FUNCTION
0	0	0	512 step update at 4 Fs, 42.6 ms at 48 kHz
0	**0**	**1**	**1024 step update at 4 Fs, 85.3 ms at 48 kHz**
0	1	0	2048 step update at 4 Fs, 170 ms at 48 kHz
0	1	1	2048 step update at 4 Fs, 170 ms at 48 kHz

Table 6–34. Treble and Bass Gain Step Size (Slew Rate)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	No operation
0	0	0	0	0	0	1	1	
0	0	0	0	0	1	0	0	Minimum rate – Updates every 0.083 ms (every LRCLK at 48 kHz)
0	0	1	0	0	0	0	0	Update ever 0.67 ms (32 LRCLKs at 48 kHz)
0	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**Default rate – Updates every 1.31 ms (63 LRCLKs at 48 kHz). This is the maximum constant time that can be set for all sample rates.**
1	1	1	1	1	1	1	1	Minimum rate – Updates every 5.08 ms (every 255 LRCLKs at 48 kHz)

6.29 Volume Registers (0xD1 – 0xD9)

Channels 1, 2, 3, 4, 5, 6, 7, and 8 are mapped into registers 0xD1, 0xD2, 0xD3, 0xD4, 0xD5, 0xD6, 0xD7, and 0xD8.

Master volume is mapped into register 0xD9.

Bits D31 – D12 are *Don't Care*.

Table 6–35. Volume Registers

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
								Unused bits

D23	D22	D21	D20	D19	D18	D17	D16	FUNCTION
								Unused bits

D15	D14	D13	D12	D11	D10	D9	D8	FUNCTION
				V11	**V10**	**V9**	**V8**	Volume

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
V7	**V6**	**V5**	**V4**	**V3**	**V2**	**V1**	**V0**	Volume

Table 6–36. Master and Individual Volume Controls

VOLUME INDEX (H)	GAIN/INDEX	EXPECTED	ACTUAL
001	17.75	17.81	17.81
002	17.5	17.56	17.56
003	17.25	17.31	17.31
004	17	17.06	17.06
005	16.75	16.81	16.81
006	16.5	16.56	16.56
007	16.25	16.31	16.31
008	16	16.05	16.05
009	15.75	15.8	15.8
00A	15.5	15.55	15.55
00B	15.25	15.3	15.3
00C	15	15.05	15.05
00D	14.75	14.8	14.8
00E	14.5	14.55	14.55
00F	14.25	14.3	14.3
010	14	14.05	14.05
044	1	1	1
045	0.75	0.75	0.75
046	0.5	0.5	0.5
047	0.25	0.25	0.25
048	0	0	0
049	–0.25	–0.25	–0.25
04A	–0.5	–0.5	–0.5
04B	–0.75	–0.75	–0.75
04C	–1	–1	–1
240	–126	–126.43	–126.43
241	–126.25	–126.68	–126.99
242	–126.5	–126.93	–126.99
243	–126.75	–127.19	–127.59
244	–127	–127.44	–127.59
245	**Mute**	**Mute**	**Mute**
TO			
3FF	**Mute**	**Mute**	**Mute**

6.30 Bass Filter Set Register (0xDA)

Bits D31–D27, D23–D19, D15–D11, and D7–D3 are *Don't Care*.

Table 6–37. Channel 8 Sub Woofer

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	0	0	0	0	0	0	0	No change
0	0	0	0	0	0	0	1	Bass filter set 1
0	0	0	0	0	0	1	0	Bass filter set 2
0	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**Bass filter set 3**
0	0	0	0	0	1	0	0	Bass filter set 4
0	0	0	0	0	1	0	1	Bass filter set 5
0	0	0	0	0	1	1	0	Illegal
0	0	0	0	0	1	1	1	Illegal

Table 6–38. Channel 6 and 5 (Right and Left Lineout in Six Channel Configuration Right and Left Surround in Eight Channel Configuration)

D23	D22	D21	D20	D19	D18	D17	D16	FUNCTION
0	0	0	0	0	0	0	0	No change
0	0	0	0	0	0	0	1	Bass filter set 1
0	0	0	0	0	0	1	0	Bass filter set 2
0	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**Bass filter set 3**
0	0	0	0	0	1	0	0	Bass filter set 4
0	0	0	0	0	1	0	1	Bass filter set 5
0	0	0	0	0	1	1	0	Illegal
0	0	0	0	0	1	1	1	Illegal

Table 6–39. Channel 4 and 3 (Right and Left Rear)

D15	D14	D13	D12	D11	D10	D9	D8	FUNCTION
0	0	0	0	0	0	0	0	No change
0	0	0	0	0	0	0	1	Bass filter set 1
0	0	0	0	0	0	1	0	Bass filter set 2
0	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**Bass filter set 3**
0	0	0	0	0	1	0	0	Bass filter set 4
0	0	0	0	0	1	0	1	Bass filter set 5
0	0	0	0	0	1	1	0	Illegal
0	0	0	0	0	1	1	1	Illegal

Table 6–40. Channel 7, 2, 1 (Center, Right Front, and Left Front)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	No change
0	0	0	0	0	0	0	1	Bass filter set 1
0	0	0	0	0	0	1	0	Bass filter set 2
0	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**Bass filter set 3**
0	0	0	0	0	1	0	0	Bass filter set 4
0	0	0	0	0	1	0	1	Bass filter set 5
0	0	0	0	0	1	1	0	Illegal
0	0	0	0	0	1	1	1	Illegal

6.31 Bass Filter Index Register (0xDB)

Index values above 0x24 are invalid.

Table 6–41. Bass Filter Index Register

I²C SUBADDRESS	TOTAL BYTES	REGISTER NAME	DESCRIPTION OF CONTENTS	DEFAULT STATE
0xDB	Bass filter index (BFI)	4	Ch8_BFI (31:24), Ch65_BFI (23:16), Ch43_BFI (15:8), Ch721_BFI (7:0)	0x12, 0x12, 0x12, 0x12,

Table 6–42. Bass Filter Index Table

TREBLE INDEX VALUE	ADJUSTMENT (DB)	TREBLE INDEX VALUE	ADJUSTMENT (DB)
0x00	+18	0x13	–1
0x01	+17	0x14	–2
0x02	+16	0x15	–3
0x03	+15	0x16	–4
0x04	+14	0x17	–5
0x05	+13	0x18	–6
0x06	+12	0x19	–7
0x07	+11	0x1A	–8
0x08	+10	0x1B	–9
0x09	+9	0x1C	–10
0x0A	+8	0x1D	–11
0x0B	+7	0x1E	–12
0x0C	+6	0x1F	–13
0x0D	+5	0x20	–14
0x0E	+4	0x21	–15
0x0F	+3	0x22	–16
0x10	+2	0x23	–17
0x11	+1	0x24	–18
0x12	**0**		

6.32 Treble Filter Set Register (0xDC)

Bits D31–D27 are *Don't Care*.

Table 6–43. Channel 8 Sub Woofer

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
0	0	0	0	0	0	0	0	No change
0	0	0	0	0	0	0	1	Treble filter set 1
0	0	0	0	0	0	1	0	Treble filter set 2
0	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**Treble filter set 3**
0	0	0	0	0	1	0	0	Treble filter set 4
0	0	0	0	0	1	0	1	Treble filter set 5
0	0	0	0	0	1	1	0	Illegal
0	0	0	0	0	1	1	1	Illegal

Table 6–44. Channel 6 and 5 (Right and Left Lineout in Six Channel Configuration or Right and Left Surround in Eight Channel Configuration)

D23	D22	D21	D20	D19	D18	D17	D16	FUNCTION
0	0	0	0	0	0	0	0	No change
0	0	0	0	0	0	0	1	Treble filter set 1
0	0	0	0	0	0	1	0	Treble filter set 2
0	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**Treble filter set 3**
0	0	0	0	0	1	0	0	Treble filter set 4
0	0	0	0	0	1	0	1	Treble filter set 5
0	0	0	0	0	1	1	0	Illegal
0	0	0	0	0	1	1	1	Illegal

Table 6–45. Channel 4 and 3 (Right and Left Rear)

D15	D14	D13	D12	D11	D10	D9	D8	FUNCTION
0	0	0	0	0	0	0	0	No change
0	0	0	0	0	0	0	1	Treble filter set 1
0	0	0	0	0	0	1	0	Treble filter set 2
0	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**Treble filter set 3**
0	0	0	0	0	1	0	0	Treble filter set 4
0	0	0	0	0	1	0	1	Treble filter set 5
0	0	0	0	0	1	1	0	Illegal
0	0	0	0	0	1	1	1	Illegal

Table 6–46. Channel 7, 2, 1 (Center, Right Front, and Left Front)

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
0	0	0	0	0	0	0	0	No change
0	0	0	0	0	0	0	1	Treble filter set 1
0	0	0	0	0	0	1	0	Treble filter set 2
0	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**Treble filter set 3**
0	0	0	0	0	1	0	0	Treble filter set 4
0	0	0	0	0	1	0	1	Treble filter set 5
0	0	0	0	0	1	1	0	Illegal
0	0	0	0	0	1	1	1	Illegal

6.33 Treble Filter Index (0xDD)

Index values above 0x24 are invalid.

Table 6–47. Treble Filter Index Register

I^2C SUBADDRESS	TOTAL BYTES	REGISTER NAME	DESCRIPTION OF CONTENTS	DEFAULT STATE
0xDD	Treble filter index (TFI)	4	Ch8_TFI (31:24), Ch65_TFI (23:16), Ch43_TFI (15:8), Ch721_TFI (7:0)	0x12,0x12,0x12,0x12

Table 6–48. Treble Filter Index

TREBLE INDEX VALUE	ADJUSTMENT (DB)	TREBLE INDEX VALUE	ADJUSTMENT (DB)
0x00	+18	0x13	–1
0x01	+17	0x14	–2
0x02	+16	0x15	–3
0x03	+15	0x16	–4
0x04	+14	0x17	–5
0x05	+13	0x18	–6
0x\06	+12	0x19	–7
0x07	+11	0x1A	–8
0x08	+10	0x1B	–9
0x09	+9	0x1C	–10
0x0A	+8	0x1D	–11
0x0B	+7	0x1E	–12
0x0C	+6	0x1F	–13
0x0D	+5	0x20	–14
0x0E	+4	0x21	–15
0x0F	+3	0x22	–16
0x10	+2	0x23	–17
0x11	+1	0x24	–18
0x12	**0**		

6.34 AM Mode Register (0xDE)

Bits D31–D21 are *Don't Care*.

Table 6–49. AM Mode Register

D31	D30	D29	D28	D27	D26	D25	D24	FUNCTION
								Unused bits

D23	D22	D21	D20	D19	D18	D17	D16	FUNCTION
			0	**–**	**–**	**–**	**–**	**AM mode disabled**
			1	–	–	–	–	AM mode enabled
			–	**0**	**0**	**–**	**–**	**Select sequence 1**
			–	0	1	–	–	Select sequence 2
			–	1	0	–	–	Select sequence 3
			–	1	1	–	–	Select sequence 4
			–	**–**	**–**	**0**	**–**	**IF frequency 455**
			–	–	–	1	–	IF frequency 262.5
			–	**–**	**–**	**–**	**0**	**Use BCD tuned frequency**
			–	–	–	–	1	Use binary tuned frequency

Table 6–50. AM Tuned Frequency Register in BCD Mode (Lower 2 Bytes of 0xDE)

D15	D14	D13	D12	D11	D10	D9	D8	FUNCTION
0	0	0	B0	–	–	–	–	BCD frequency (1000s kHz)
–	–	–	–	B3	B2	B1	B0	BCD frequency (100s kHz)
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Default value**

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
B3	B2	B1	B0	–	–	–	–	BCD frequency (10s kHz)
–	–	–	–	B3	B2	B1	B0	BCD frequency (1s kHz)
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Default value**

Table 6–51. AM Tuned Frequency Register in Binary Mode (Lower 2 Bytes of 0xDE)

D15	D14	D13	D12	D11	D10	D9	D8	FUNCTION
0	0	0	0	0	B10	B9	B8	Binary frequency (upper 3 bits)
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Default value**

D7	D6	D5	D4	D3	D2	D1	D0	FUNCTION
B7	B6	B5	B4	B3	B2	B1	B0	Binary frequency (lower 8 bits)
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**Default value**

6.35 PSVC Range Register (0xDF)

Bits D31–D2 are zero.

Table 6–52. PSVC Range Register

D31 – D2	D1	D0	FUNCTION
0	**0**	**0**	**12.04-dB control range for PSVC**
0	0	1	18.06-dB control range for PSVC
0	1	0	24.08-dB control range for PSVC
0	1	1	Ignore – retain last value

6.36 General Control Register (0xE0)

Bits D31–D4 are zero. Bit D0 is *Don't Care*.

Table 6–53. General Control Register

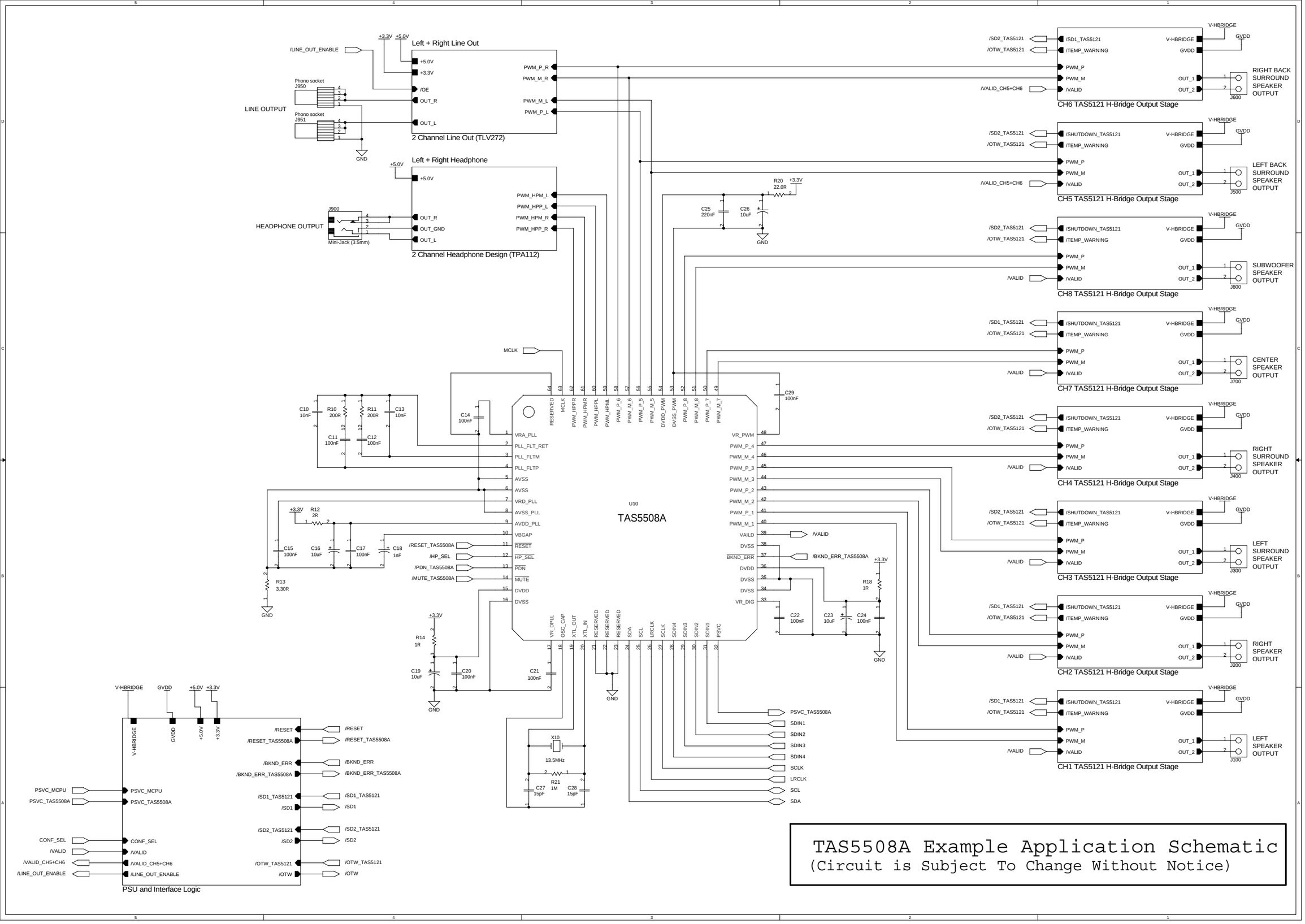
D31 – D4	D3	D2	D1	D0	FUNCTION
0		**–**	**0**		**8 channel configuration**
0		–	1		6 channel configuration
0		**0**	**–**		**Power supply volume control disable**
0		1	–		Power supply volume control enable
0	**0**	**–**	**–**		**Subwoofer part of PSVC (D3 is a write-only bit)**
0	1	–	–		Subwoofer separate from PSVC

6.37 Incremental Multiple Write Append Register (0xFE)

This is a special register used to append data to a previously opened register.

7 TAS5508A Example Application Schematic

The following page contains an example application schematic for the TAS5508A.



TAS5508A Example Application Schematic

(Circuit is Subject To Change Without Notice)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TAS5508APAG	NRND	TQFP	PAG	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR
TAS5508APAGG4	NRND	TQFP	PAG	64	160	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR
TAS5508APAGR	NRND	TQFP	PAG	64	1500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR
TAS5508APAGRG4	NRND	TQFP	PAG	64	1500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

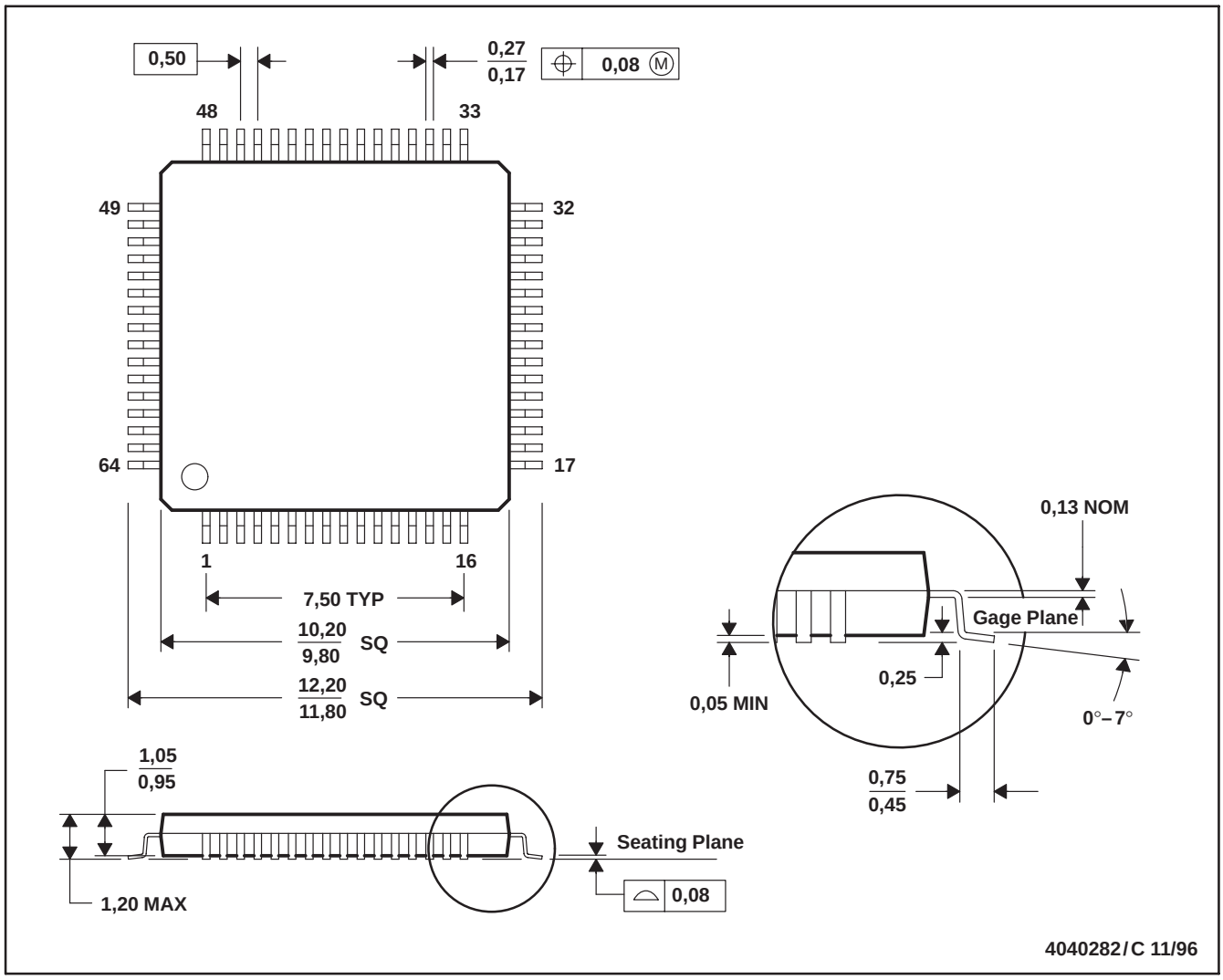
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PAG (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026