High Voltage, High and Low Side Driver

NCP5106A, NCP5106B

The NCP5106 is a high voltage gate driver IC providing two outputs for direct drive of 2 N−channel power MOSFETs or IGBTs arranged in a half−bridge configuration version B or any other high−side + low−side configuration version A.

It uses the bootstrap technique to ensure a proper drive of the high−side power switch. The driver works with 2 independent inputs.

Features

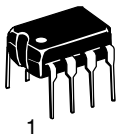
- High Voltage Range: Up to 600 V
- dV/dt Immunity ±50 V/nsec
- Negative Current Injection Characterized Over the Temperature Range
- Gate Drive Supply Range from 10 V to 20 V
- High and Low Drive Outputs
- Output Source / Sink Current Capability 250 mA / 500 mA
- 3.3 V and 5 V Input Logic Compatible
- Up to V_{CC} Swing on Input Pins
- Extended Allowable Negative Bridge Pin Voltage Swing to −10 V for Signal Propagation
- Matched Propagation Delays Between Both Channels
- Outputs in Phase with the Inputs
- Independent Logic Inputs to Accommodate All Topologies (Version A)
- Cross Conduction Protection with 100 ns Internal Fixed Dead Time (Version B)
- Under V_{CC} LockOut (UVLO) for Both Channels
- Pin−to−Pin Compatible with Industry Standards
- These are Pb−Free Devices

Typical Applications

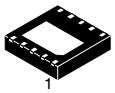
- Half−Bridge Power Converters
- Any Complementary Drive Converters (Asymmetrical Half−Bridge, Active Clamp) (A Version Only).
- Full−Bridge Converters



SOIC−8
D SUFFIX
CASE 751

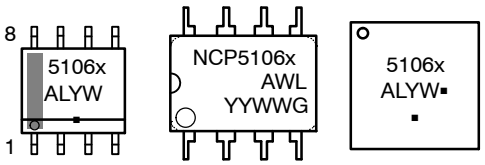


PDIP−8
P SUFFIX
CASE 626



DFN10
MN SUFFIX
CASE 506DJ

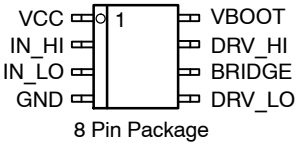
MARKING DIAGRAM



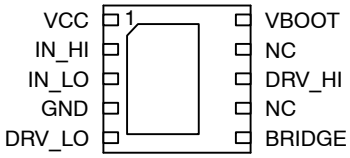
NCP5106	= Specific Device Code
x	= A or B version
A	= Assembly Location
L or WL	= Wafer Lot
Y or YY	= Year
W or WW	= Work Week
G or ▪	= Pb−Free Package

(Note: Microdot may be in either location)

PINOUT INFORMATION



8 Pin Package



10 Pin DFN Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 17 of this data sheet.

NOTE: Some of the device on this data sheet have been **DISCONTINUED**. Please refer to the table on page 17

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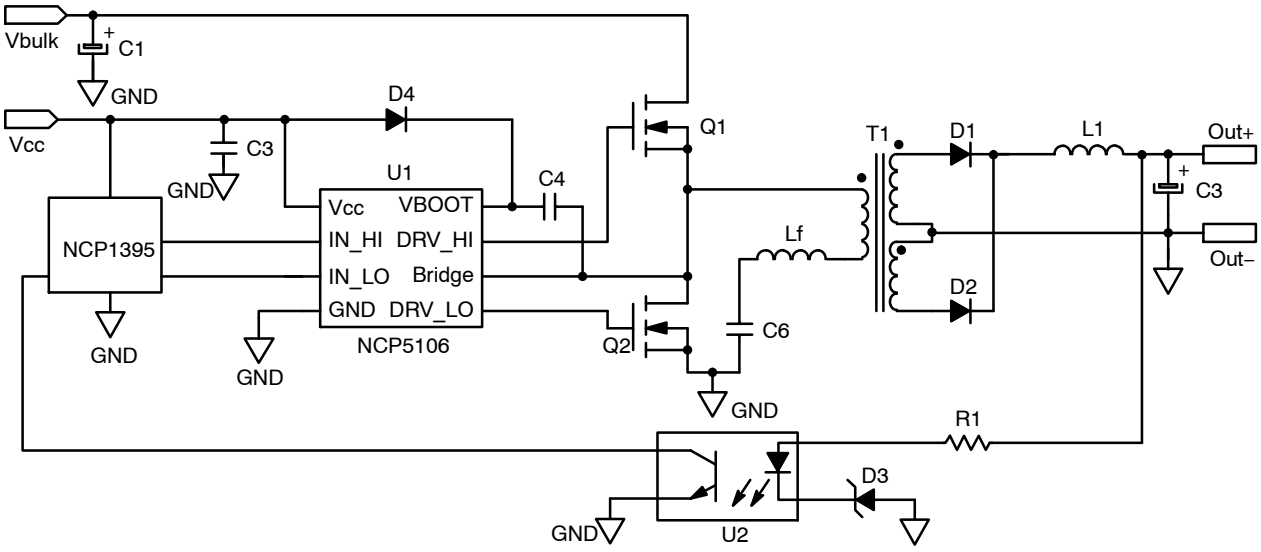


Figure 1. Typical Application Resonant Converter (LLC type)

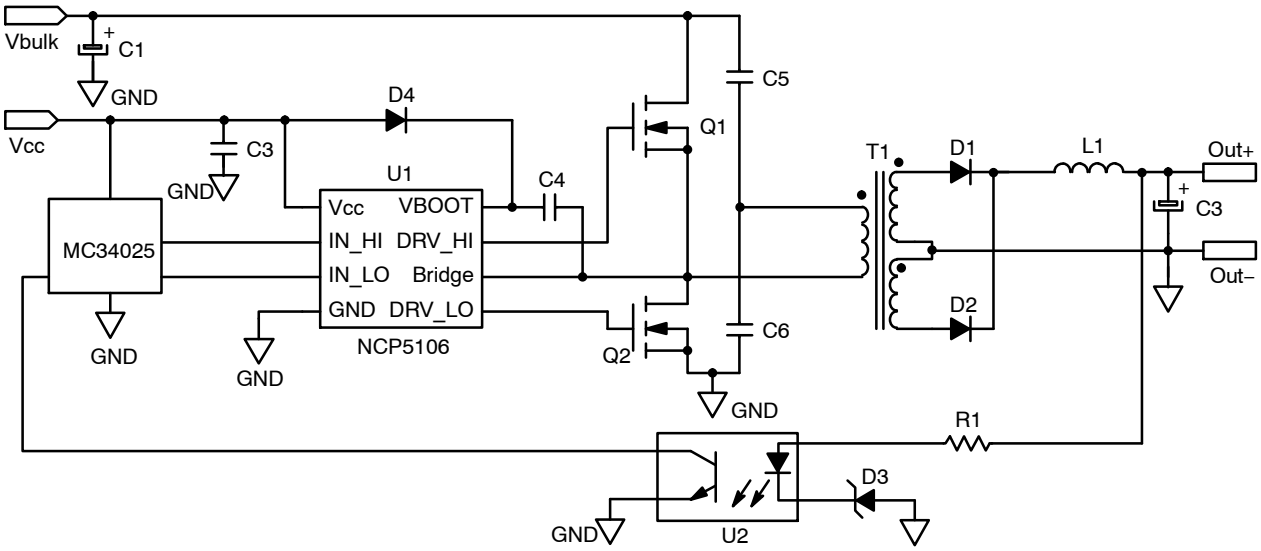


Figure 2. Typical Application Half Bridge Converter

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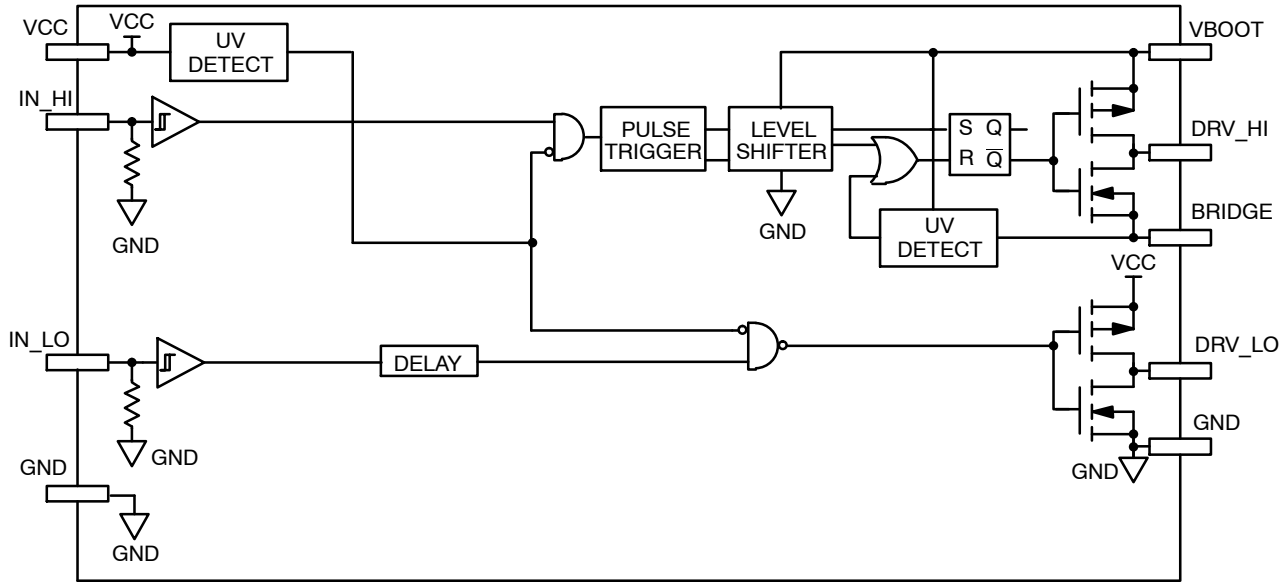


Figure 3. Detailed Block Diagram: Version A

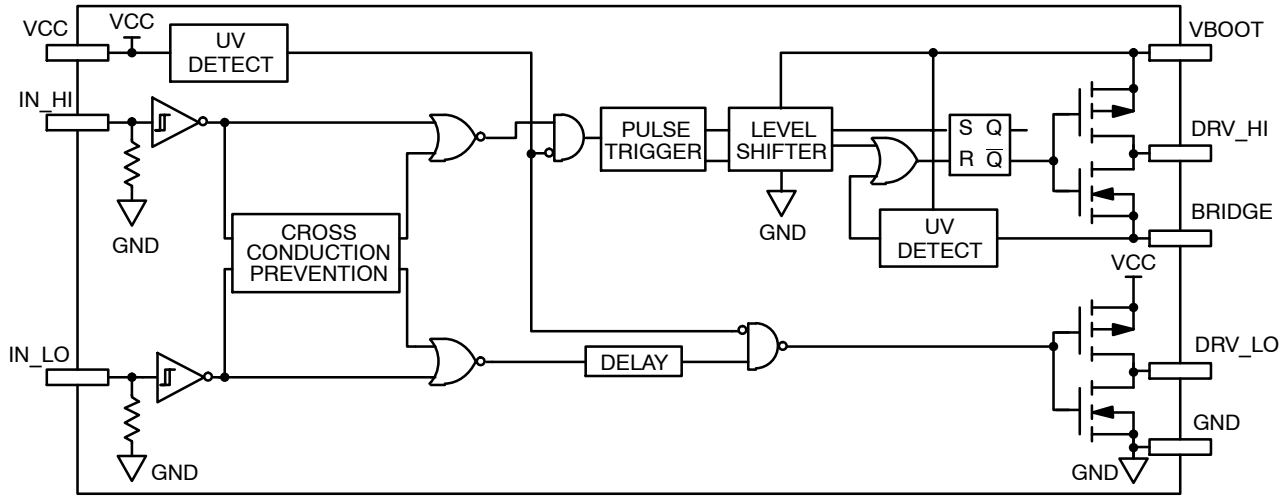


Figure 4. Detailed Block Diagram: Version B

PIN DESCRIPTION

Pin Name	Description
IN_HI	Logic Input for High Side Driver Output in Phase
IN_LO	Logic Input for Low Side Driver Output in Phase
GND	Ground
DRV_LO	Low Side Gate Drive Output
V_{CC}	Low Side and Main Power Supply
V_{BOOT}	Bootstrap Power Supply
DRV_HI	High Side Gate Drive Output
BRIDGE	Bootstrap Return or High Side Floating Supply Return
NC	Removed for creepage distance (DFN package only)

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
V_{CC}	Main power supply voltage	−0.3 to 20	V
$V_{CC_transient}$	Main transient power supply voltage: IV_{CC_max} = 5 mA during 10 ms	23	V
V_{BRIDGE}	VHV: High Voltage BRIDGE pin	−1 to 600	V
V_{BRIDGE}	Allowable Negative Bridge Pin Voltage for IN_LO Signal Propagation to DRV_LO (see characterization curves for detailed results)	−10	V
V_{BOOT}−V_{BRIDGE}	VHV: Floating supply voltage	−0.3 to 20	V
V_{DRV_HI}	VHV: High side output voltage	V_{BRIDGE} − 0.3 to V_{BOOT} + 0.3	V
V_{DRV_LO}	Low side output voltage	−0.3 to V_{CC} + 0.3	V
dV_{BRIDGE}/dt	Allowable output slew rate	50	V/ns
V_{IN_XX}	Inputs IN_HI, IN_LO	−1.0 to V_{CC} + 0.3	V
	ESD Capability: − HBM model (all pins except pins 6−7−8 in 8 pins package or 11−12−13 in 14 pins package) − Machine model (all pins except pins 6−7−8 in 8 pins package or 11−12−13 in 14 pins package)	 2 200	 kV V
	Latch up capability per JEDEC JESD78		
$R_{\theta JA}$	Power dissipation and Thermal characteristics PDIP−8: Thermal Resistance, Junction−to−Air SO−8: Thermal Resistance, Junction−to−Air DFN10 4x4: Thermal Resistance, Junction−to−Ambient 1 Oz Cu 50 mm^2 Printed Circuit Copper Clad	 100 178 162	°C/W
T_{ST}	Storage Temperature Range	−55 to +150	°C
T_{J_max}	Maximum Operating Junction Temperature	+150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

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ELECTRICAL CHARACTERISTIC (V_{CC} = V_{boot} = 15 V, V_{GND} = V_{bridge}, −40°C < T_J < 125°C, Outputs loaded with 1 nF)

Rating	Symbol	T_J −40°C to 125°C Min	Typ	Max	Units
OUTPUT SECTION					
Output high short circuit pulsed current V_{DRV} = 0 V, PW ≤ 10 μs (Note 1)	$I_{DRVsource}$	–	250	–	mA
Output low short circuit pulsed current V_{DRV} = V_{CC}, PW ≤ 10 μs (Note 1)	$I_{DRVsink}$	–	500	–	mA
Output resistor (Typical value @ 25°C) Source	R_{OH}	–	30	60	Ω
Output resistor (Typical value @ 25°C) Sink	R_{OL}	–	10	20	Ω
High level output voltage, V_{BIAS}−V_{DRV_XX} @ I_{DRV_XX} = 20 mA	V_{DRV_H}	–	0.7	1.6	V
Low level output voltage V_{DRV_XX} @ I_{DRV_XX} = 20 mA	V_{DRV_L}	–	0.2	0.6	V
DYNAMIC OUTPUT SECTION					
Turn−on propagation delay (Vbridge = 0 V)	t_{ON}	–	100	170	ns
Turn−off propagation delay (Vbridge = 0 V or 50 V) (Note 2)	t_{OFF}	–	100	170	ns
Output voltage rise time (from 10% to 90% @ V_{CC} = 15 V) with 1 nF load	tr	–	85	160	ns
Output voltage fall time (from 90% to 10% @V_{CC} = 15 V) with 1 nF load	tf	–	35	75	ns
Propagation delay matching between the High side and the Low side @ 25°C (Note 3)	Δt	–	20	35	ns
Internal fixed dead time (only valid for B version) (Note 4)	DT	65	100	190	ns
Minimum input width that changes the output	t_{PW1}	–	–	50	ns
Maximum input width that does not change the output SOIC−8, PDIP−8 DFN10	t_{PW2}	20 15	– –	– –	ns
INPUT SECTION					
Low level input voltage threshold	V_{IN}	–	–	0.8	V
Input pull−down resistor (V_{IN} < 0.5 V)	R_{IN}	–	200	–	kΩ
High level input voltage threshold	V_{IN}	2.3	–	–	V
Logic “1” input bias current @ V_{IN_XX} = 5 V @ 25°C	I_{IN+}	–	5	25	μA
Logic “0” input bias current @ V_{IN_XX} = 0 V @ 25°C	I_{IN-}	–	–	2.0	μA
SUPPLY SECTION					
V_{CC} UV Start−up voltage threshold	V_{CC}_stup	8.0	8.9	9.9	V
V_{CC} UV Shut−down voltage threshold	V_{CC}_shtdwn	7.3	8.2	9.1	V
Hysteresis on V_{CC}	V_{CC}_hyst	0.3	0.7	–	V
Vboot Start−up voltage threshold reference to bridge pin (Vboot_stup = Vboot − Vbridge)	Vboot_stup	8.0	8.9	9.9	V
Vboot UV Shut−down voltage threshold	Vboot_shtdwn	7.3	8.2	9.1	V
Hysteresis on Vboot	Vboot_hyst	0.3	0.7	–	V
Leakage current on high voltage pins to GND (V_{BOOT} = V_{BRIDGE} = DRV_HI = 600 V)	I_{HV_LEAK}	–	5	40	μA
Consumption in active mode (V_{CC} = Vboot, fsw = 100 kHz and 1 nF load on both driver outputs)	ICC1	–	4	5	mA
Consumption in inhibition mode (V_{CC} = Vboot)	ICC2	–	250	400	μA
V_{CC} current consumption in inhibition mode	ICC3	–	200	–	μA
Vboot current consumption in inhibition mode	ICC4	–	50	–	μA

1. Parameter guaranteed by design.
2. Turn−off propagation delay @ Vbridge = 600 V is guaranteed by design.
3. See characterization curve for Δt parameters variation on the full range temperature.
4. Version B integrates a dead time in order to prevent any cross conduction between DRV_HI and DRV_LO. See timing diagram of Figure 10.
5. Timing diagram definition see: Figure 7, Figure 8 and Figure 9.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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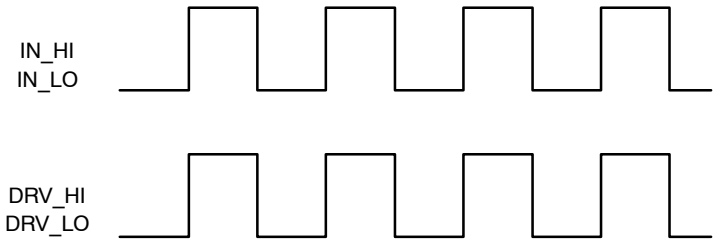


Figure 5. Input/Output Timing Diagram (A Version)

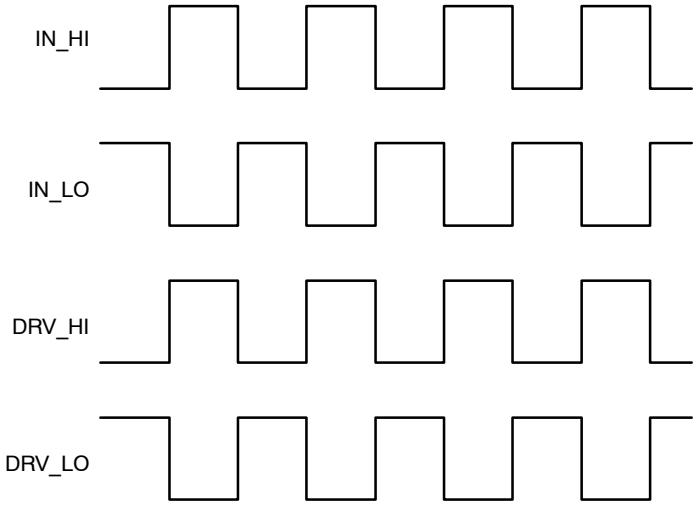


Figure 6. Input/Output Timing Diagram (B Version)

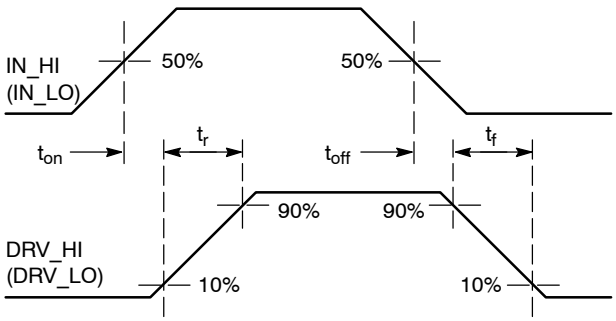


Figure 7. Propagation Delay and Rise / Fall Time Definition

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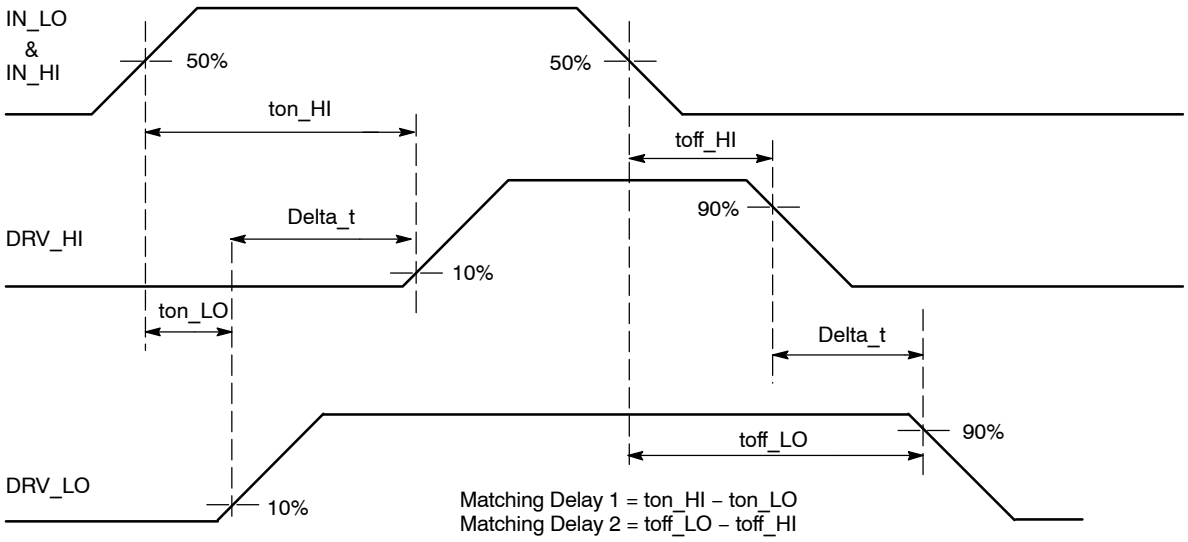


Figure 8. Matching Propagation Delay (A Version)

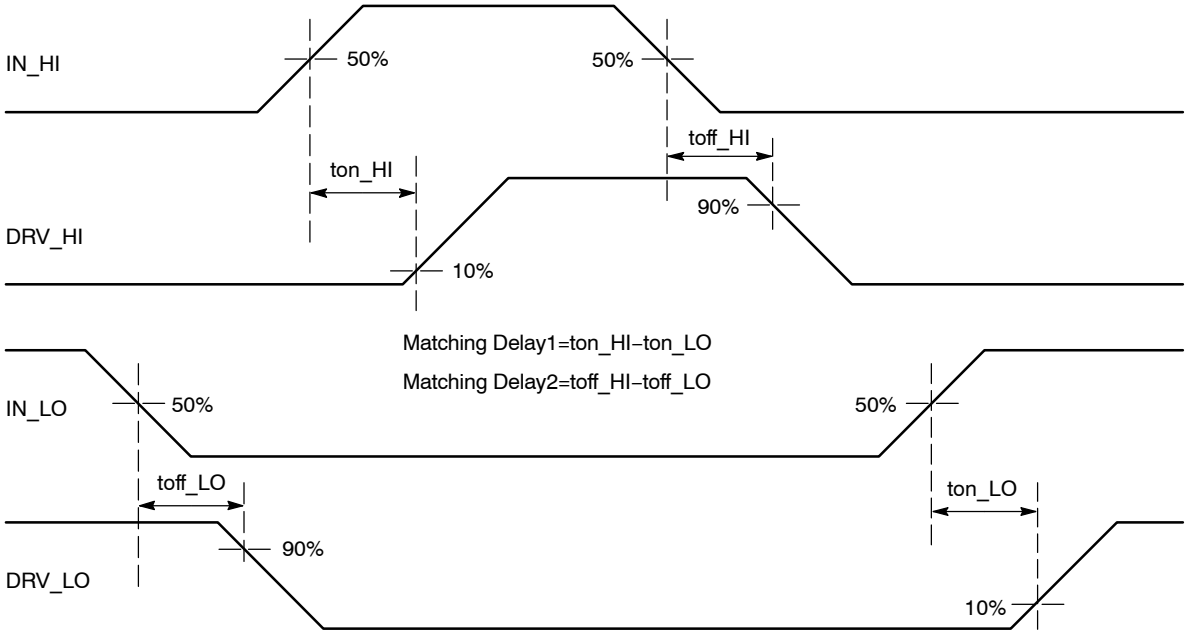


Figure 9. Matching Propagation Delay (B Version)

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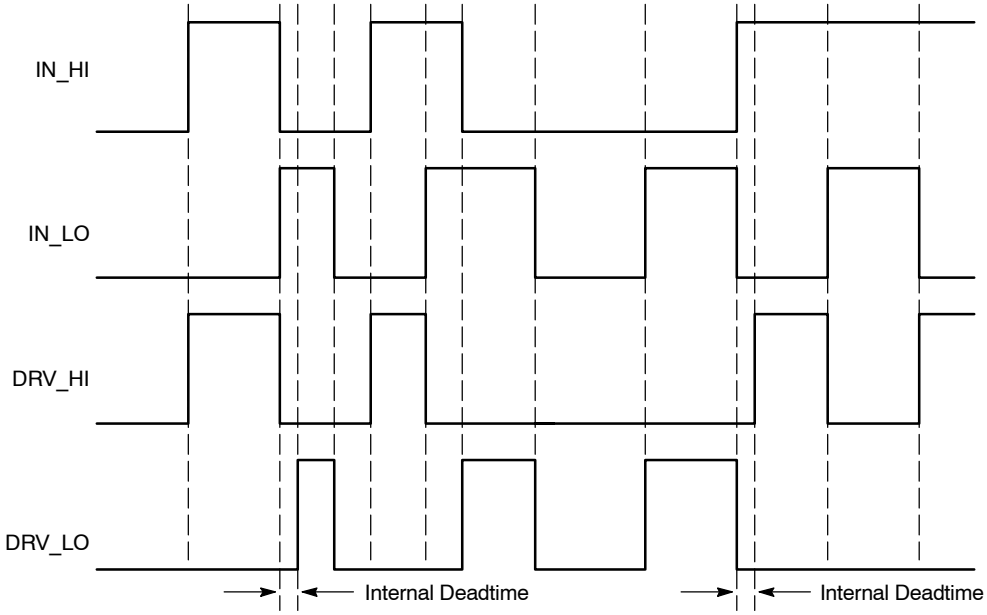


Figure 10. Input/Output Cross Conduction Output Protection Timing Diagram (B Version)

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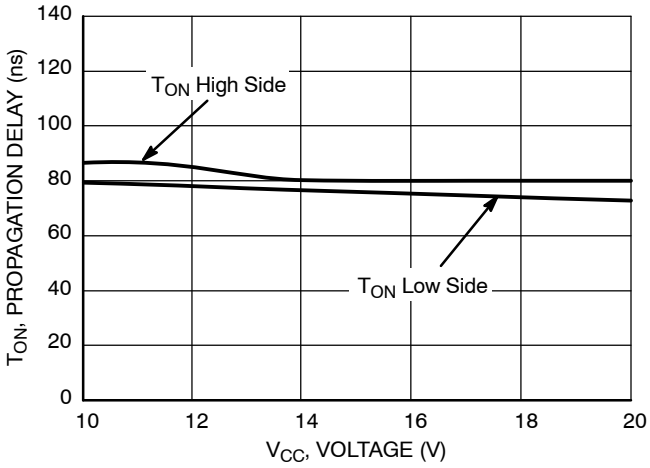


Figure 11. Turn ON Propagation Delay vs. Supply Voltage (V_{CC} = V_{BOOT})

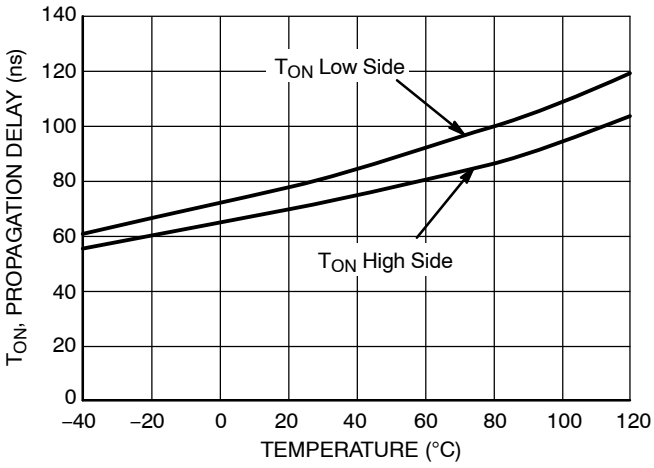


Figure 12. Turn ON Propagation Delay vs. Temperature

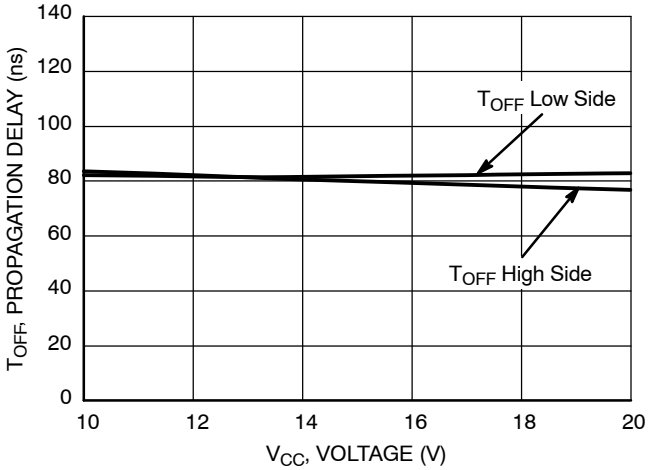


Figure 13. Turn OFF Propagation Delay vs. Supply Voltage (V_{CC} = V_{BOOT})

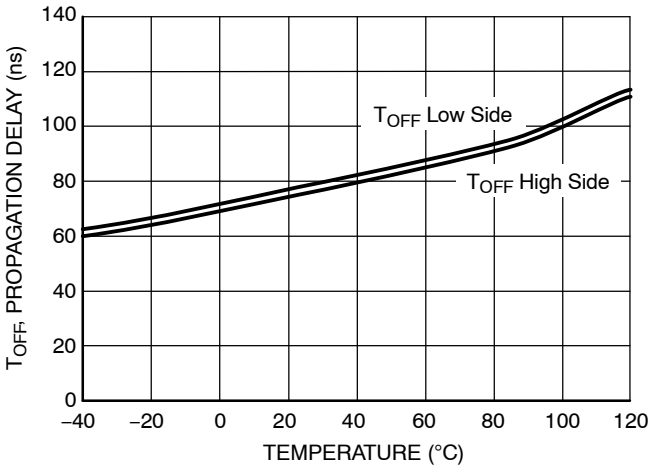


Figure 14. Turn OFF Propagation Delay vs. Temperature

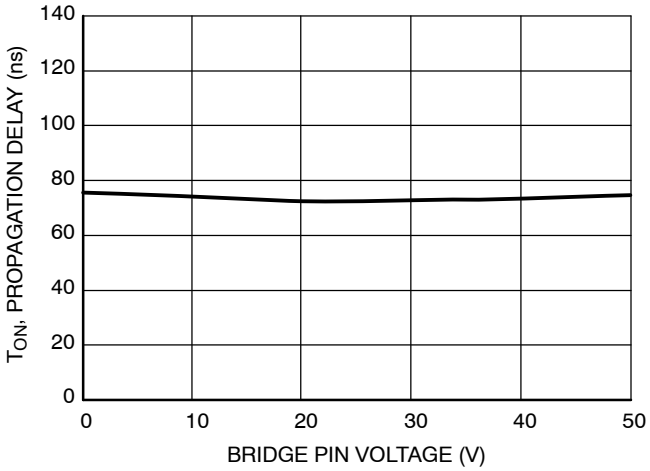


Figure 15. High Side Turn ON Propagation Delay vs. VBRIDGE Voltage

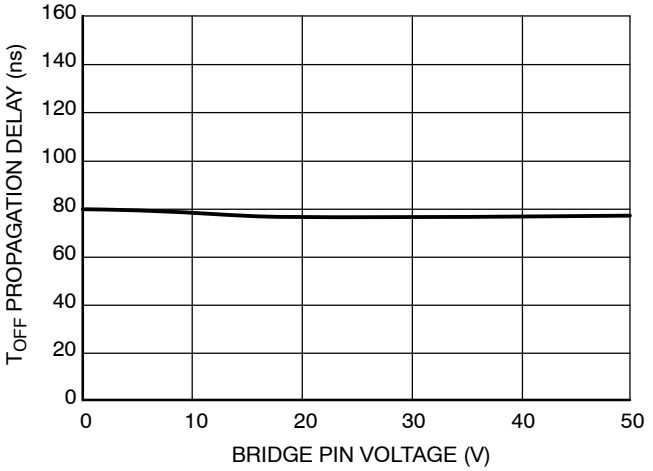


Figure 16. High Side Turn OFF Propagation Delay vs. VBRIDGE Voltage

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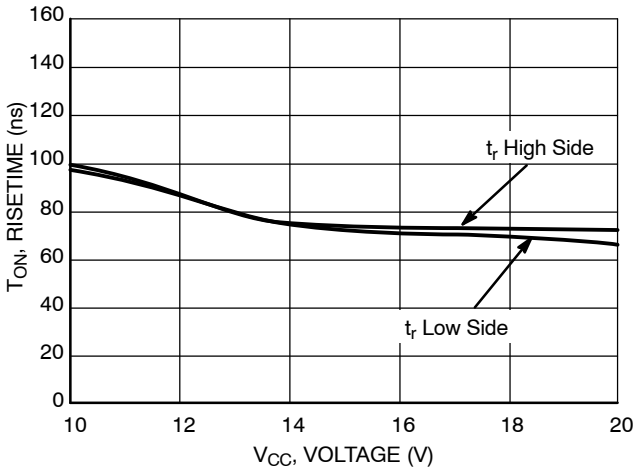


Figure 17. Turn ON Risetime vs. Supply Voltage (V_{CC} = V_{BOOT})

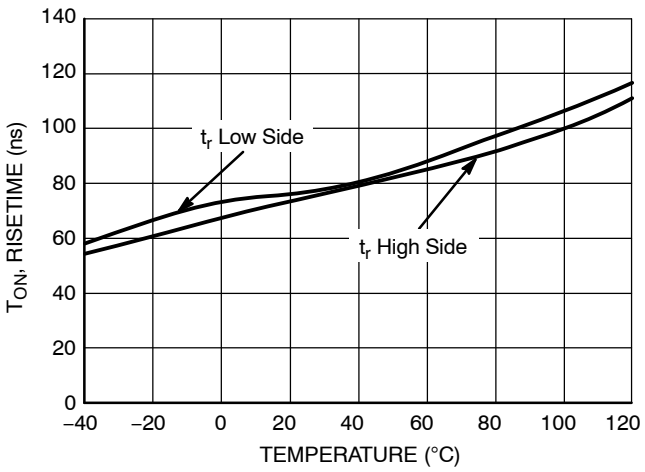


Figure 18. Turn ON Risetime vs. Temperature

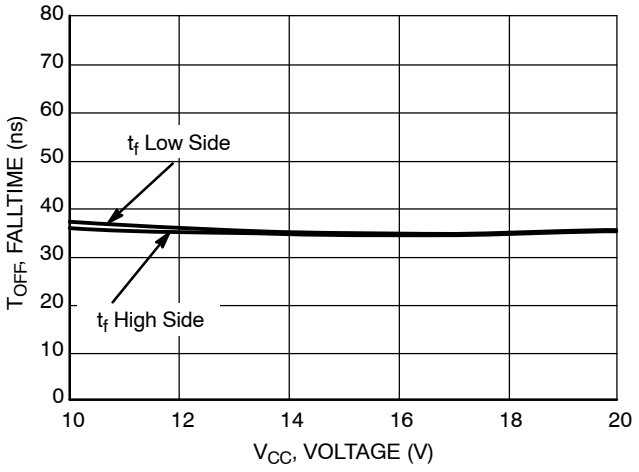


Figure 19. Turn OFF Falltime vs. Supply Voltage (V_{CC} = V_{BOOT})

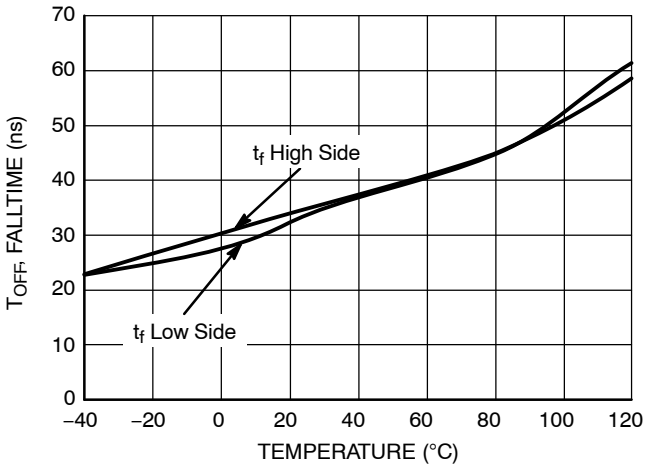


Figure 20. Turn OFF Falltime vs. Temperature

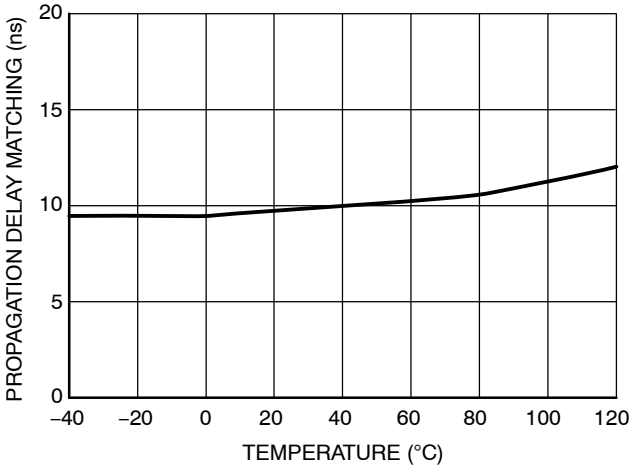


Figure 21. Propagation Delay Matching Between High Side and Low Side Driver vs. Temperature

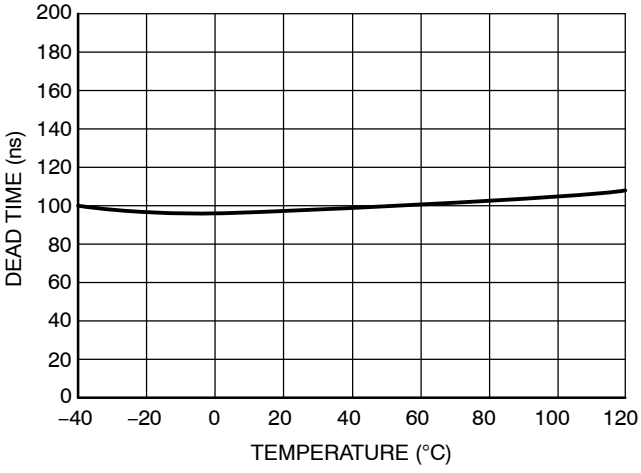


Figure 22. Dead Time vs. Temperature

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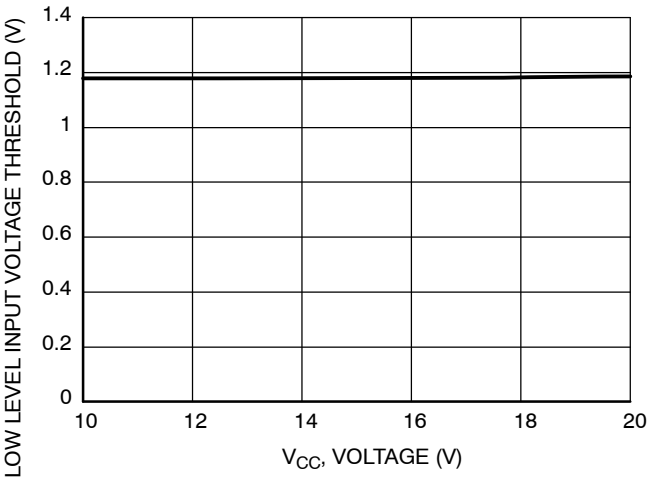


Figure 23. Low Level Input Voltage Threshold vs. Supply Voltage (V_{CC} = V_{BOOT})

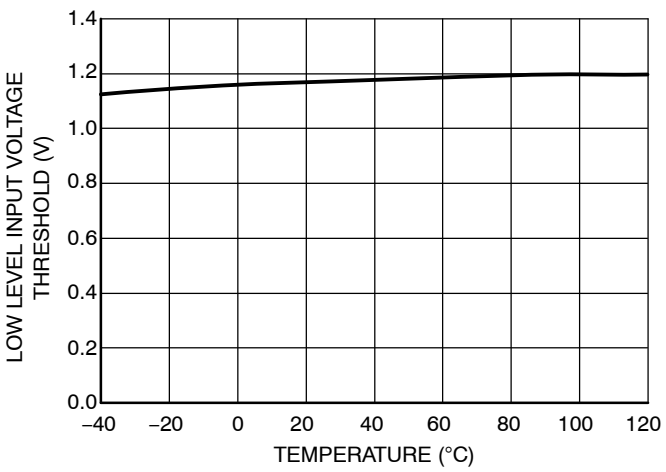


Figure 24. Low Level Input Voltage Threshold vs. Temperature

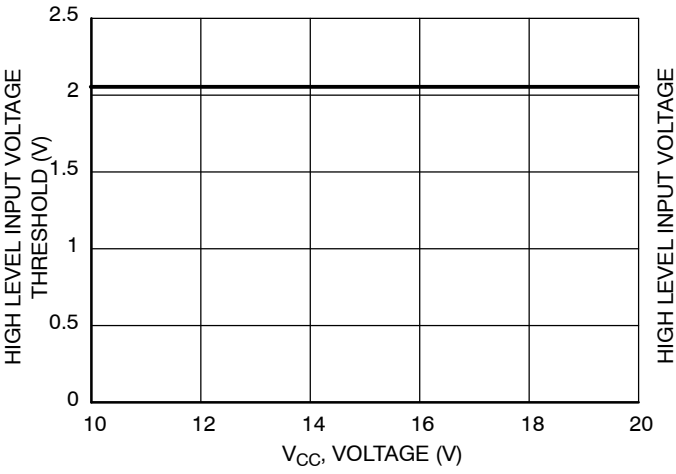


Figure 25. High Level Input Voltage Threshold vs. Supply Voltage (V_{CC} = V_{BOOT})

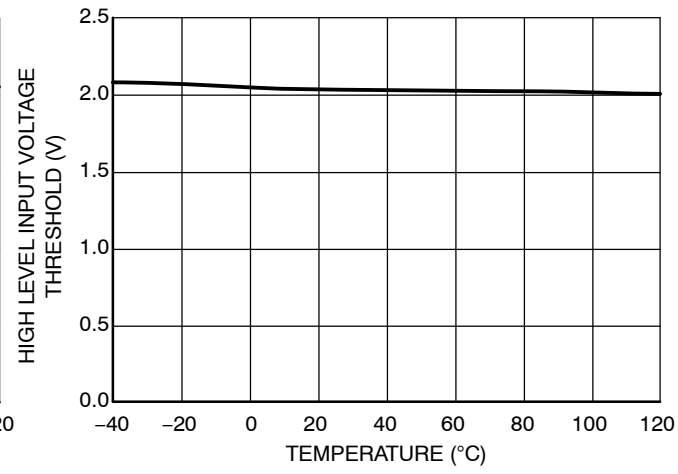


Figure 26. High Level Input Voltage Threshold vs. Temperature

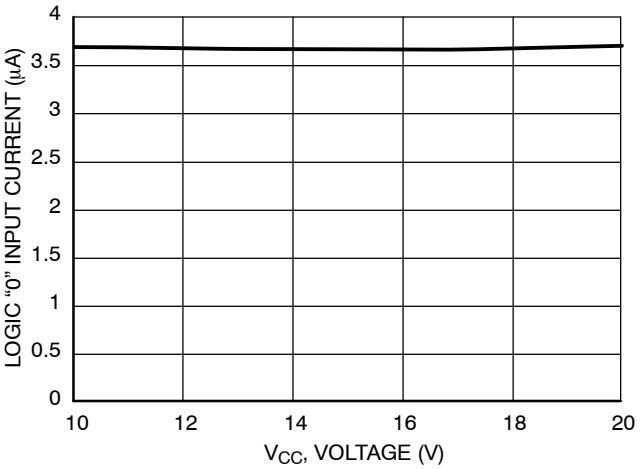


Figure 27. Logic "0" Input Current vs. Supply Voltage (V_{CC} = V_{BOOT})

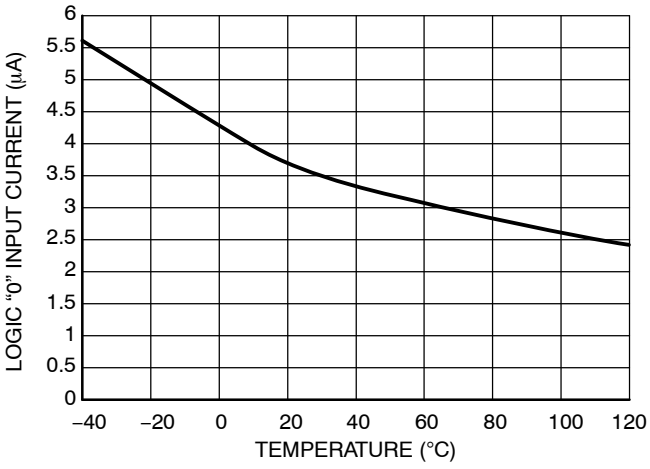


Figure 28. Logic "0" Input Current vs. Temperature

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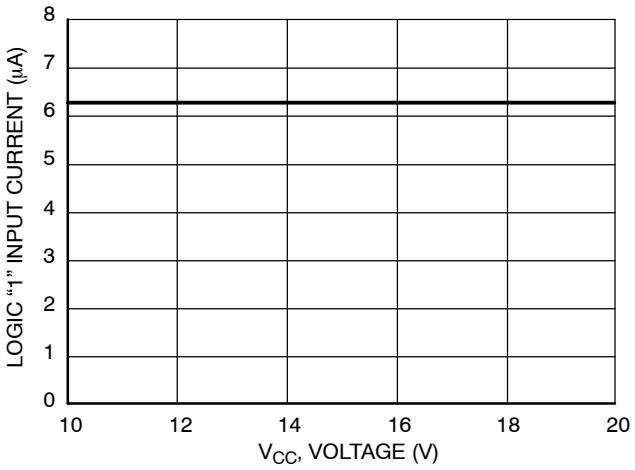


Figure 29. Logic "1" Input Current vs. Supply Voltage (V_{CC} = V_{BOOT})

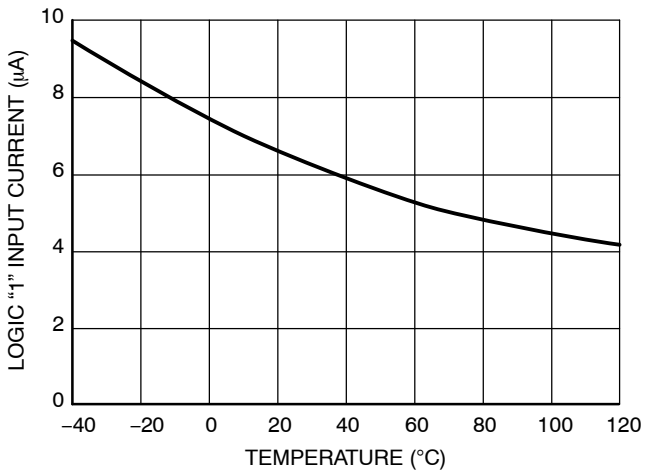


Figure 30. Logic "1" Input Current vs. Temperature

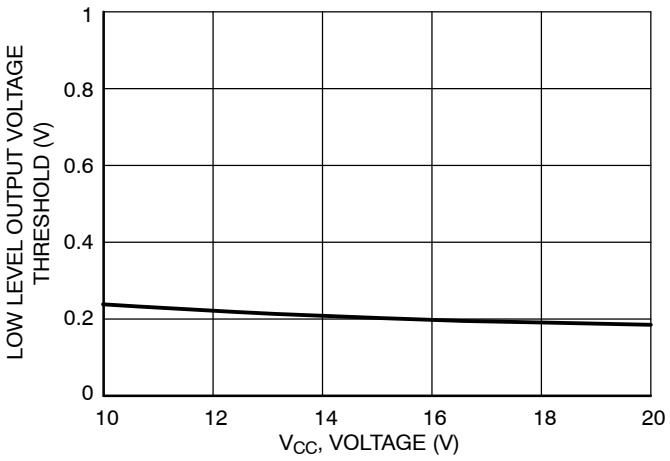


Figure 31. Low Level Output Voltage vs. Supply Voltage (V_{CC} = V_{BOOT})

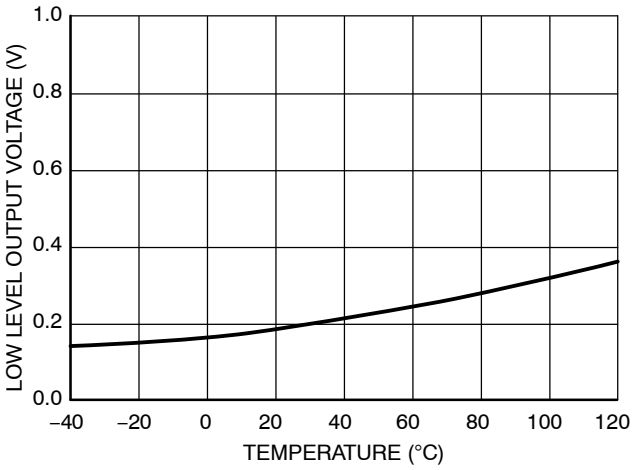


Figure 32. Low Level Output Voltage vs. Temperature

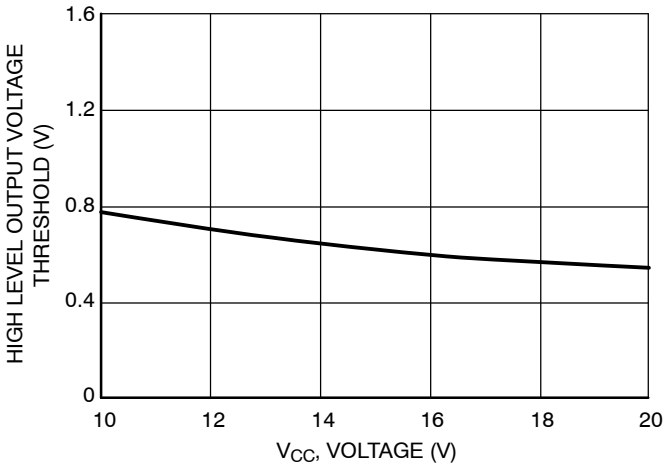


Figure 33. High Level Output Voltage vs. Supply Voltage (V_{CC} = V_{BOOT})

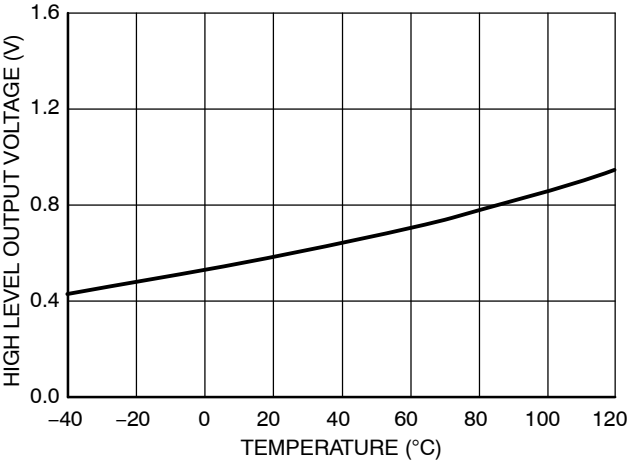


Figure 34. High Level Output Voltage vs. Temperature

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CHARACTERIZATION CURVES

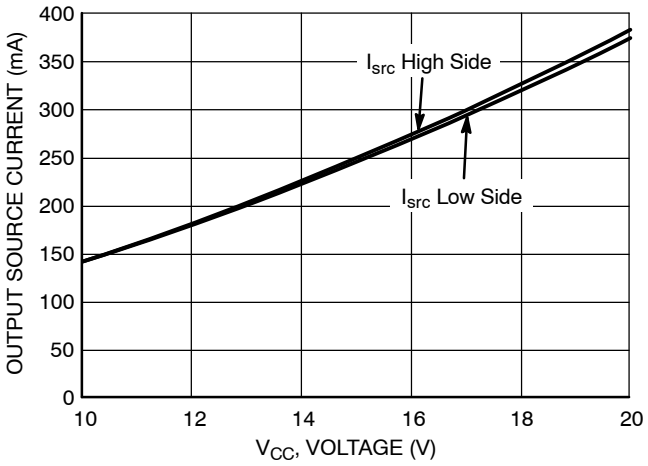


Figure 35. Output Source Current vs. Supply Voltage (V_{CC} = V_{BOOT})

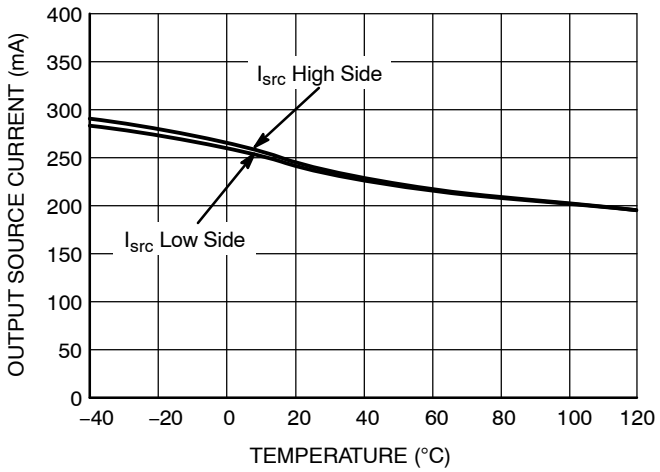


Figure 36. Output Source Current vs. Temperature

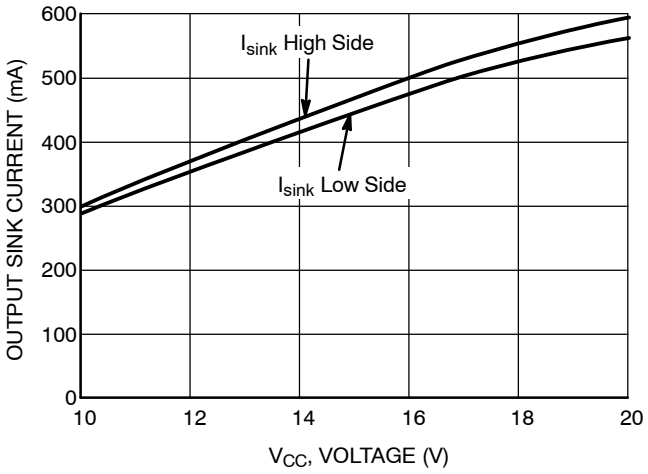


Figure 37. Output Sink Current vs. Supply Voltage (V_{CC} = V_{BOOT})

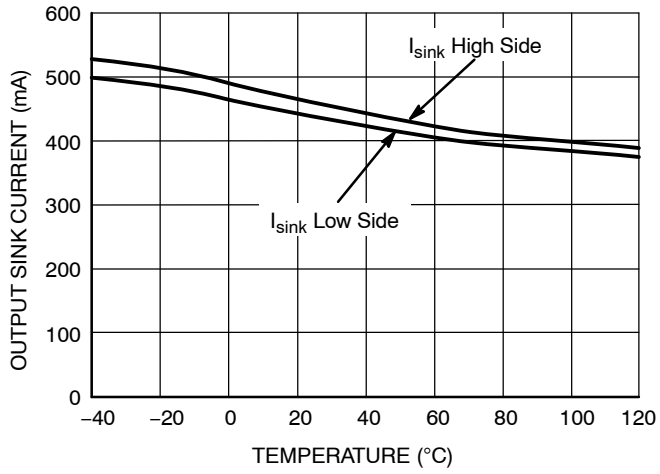


Figure 38. Output Sink Current vs. Temperature

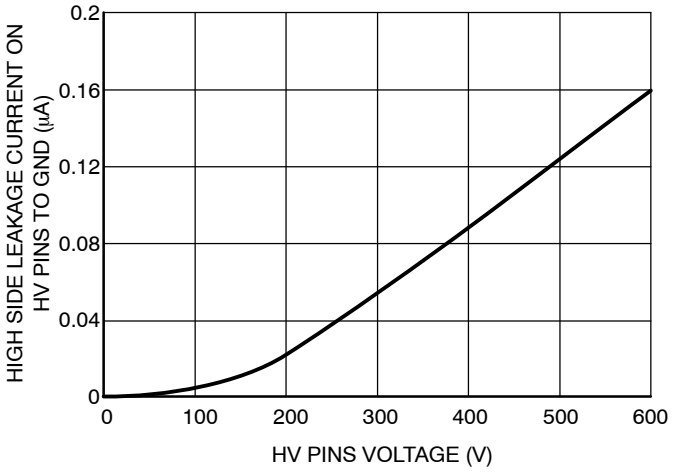


Figure 39. Leakage Current on High Voltage Pins (600 V) to Ground vs. V_{BRIDGE} Voltage (V_{BRIGDE} = V_{BOOT} = $V_{DRV\ HI}$)

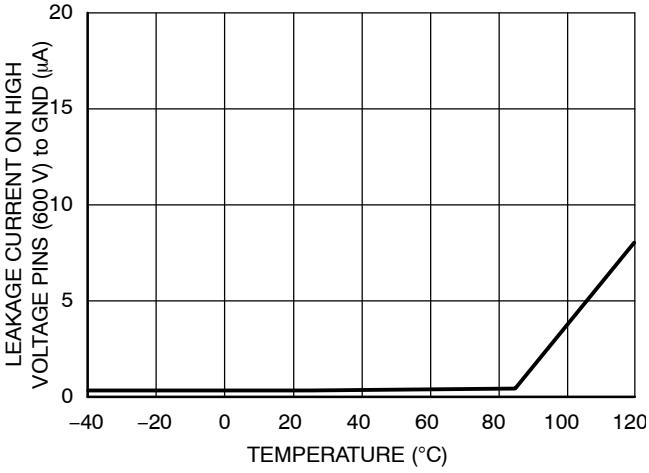


Figure 40. Leakage Current on High Voltage Pins (600 V) to Ground vs. Temperature (VBRIDGE = V_{BOOT} = $V_{DRv\ HI}$ = 600 V)

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CHARACTERIZATION CURVES

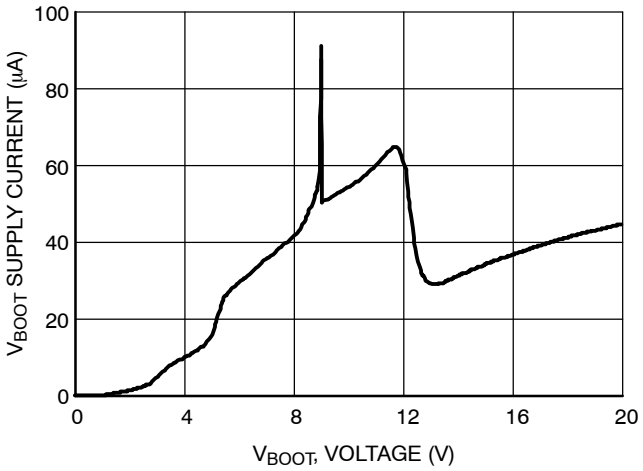


Figure 41. V_{BOOT} Supply Current vs. Bootstrap Supply Voltage

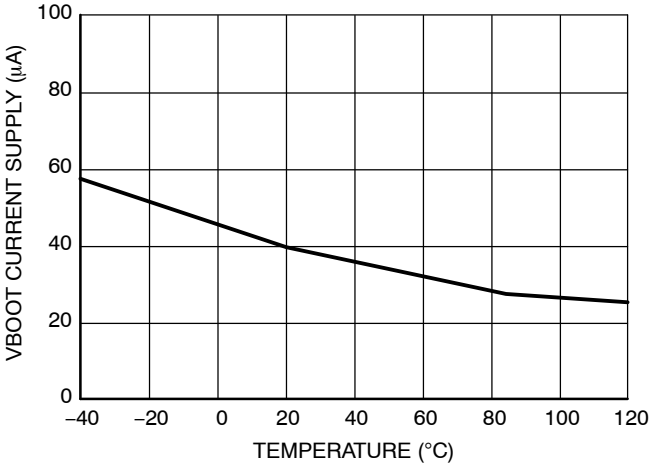


Figure 42. V_{BOOT} Supply Current vs. Temperature

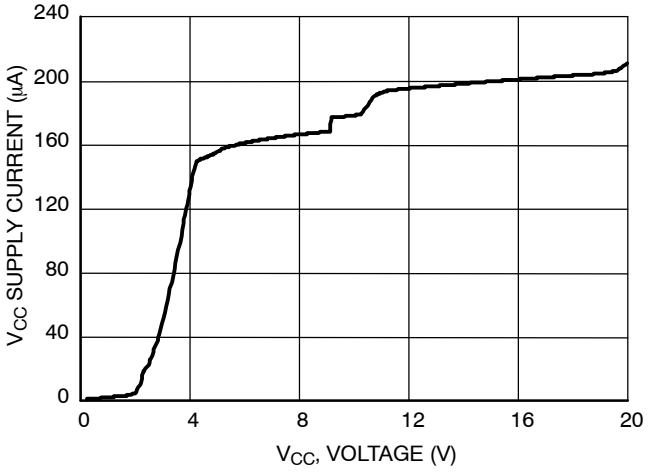


Figure 43. V_{CC} Supply Current vs. V_{CC} Supply Voltage

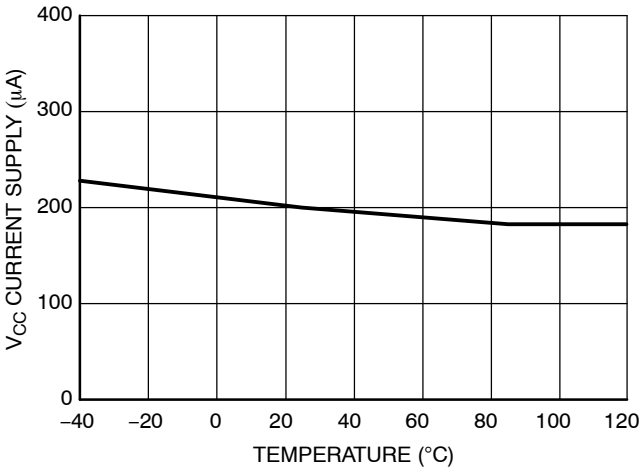


Figure 44. V_{CC} Supply Current vs. Temperature

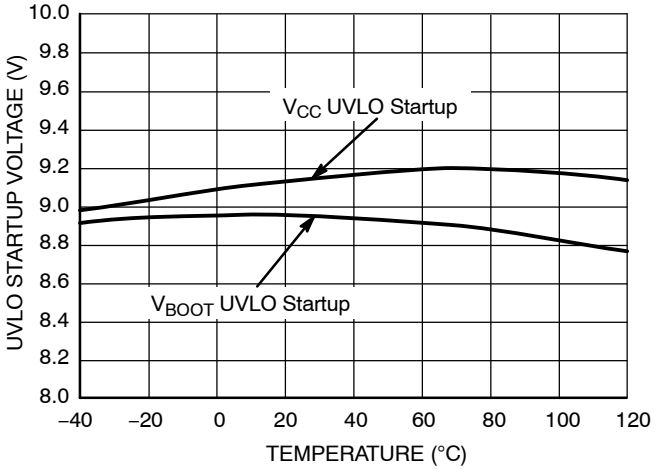


Figure 45. UVLO Startup Voltage vs. Temperature

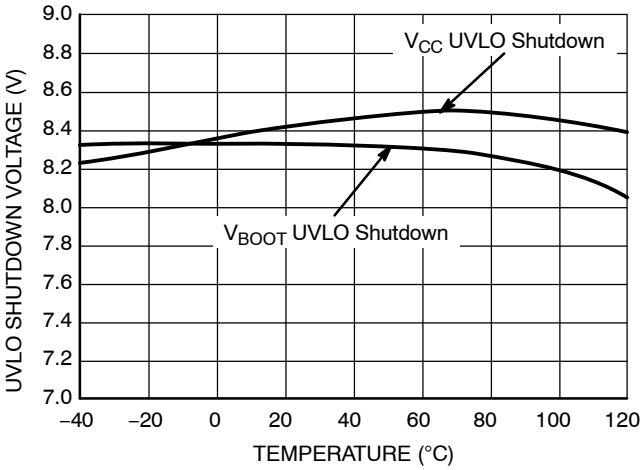


Figure 46. UVLO Shutdown Voltage vs. Temperature

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CHARACTERIZATION CURVES

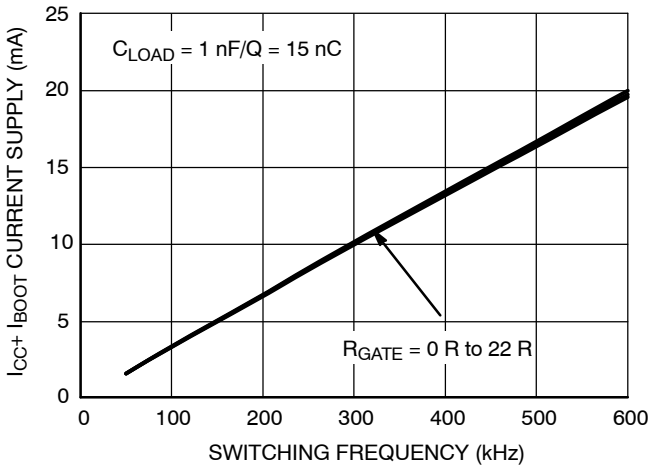


Figure 47. I_{CC1} Consumption vs. Switching Frequency with 15 nC Load on Each Driver @ V_{CC} = 15 V

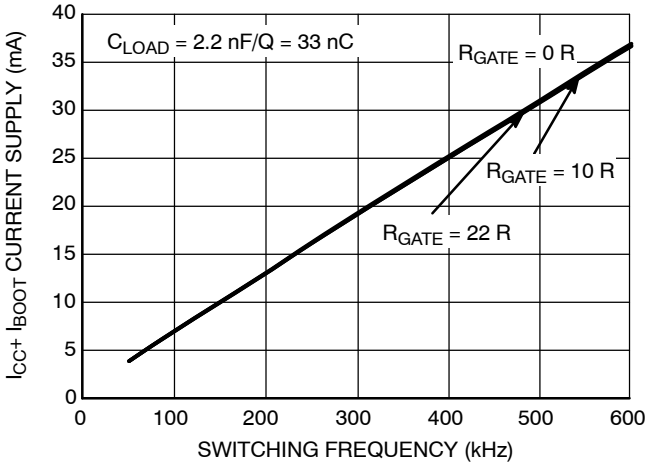


Figure 48. I_{CC1} Consumption vs. Switching Frequency with 33 nC Load on Each Driver @ V_{CC} = 15 V

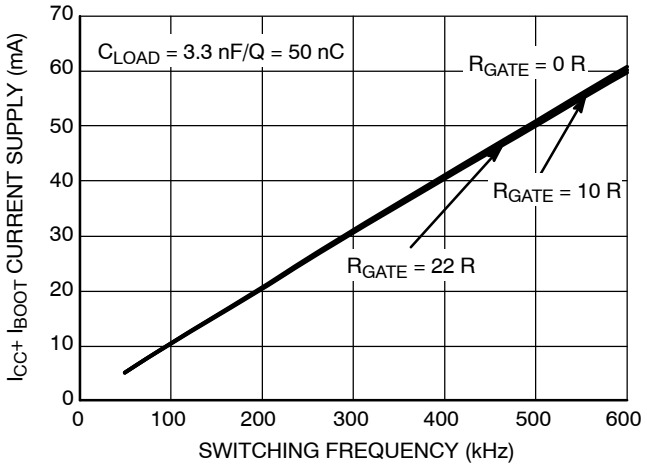


Figure 49. I_{CC1} Consumption vs. Switching Frequency with 50 nC Load on Each Driver @ V_{CC} = 15 V

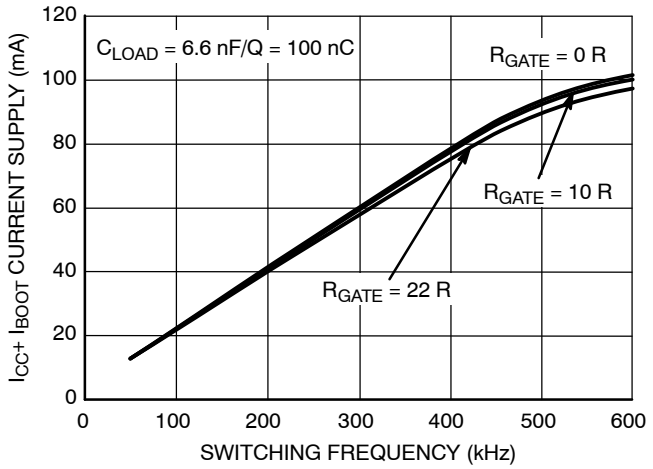


Figure 50. I_{CC1} Consumption vs. Switching Frequency with 100 nC Load on Each Driver @ V_{CC} = 15 V

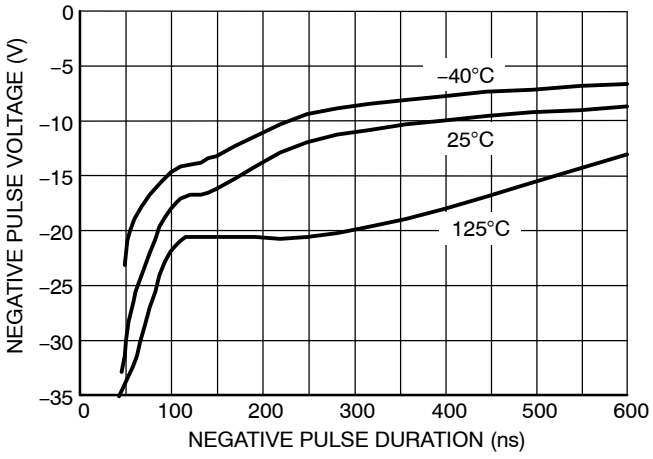


Figure 51. NCP5106A, Negative Voltage Safe Operating Area on the Bridge Pin

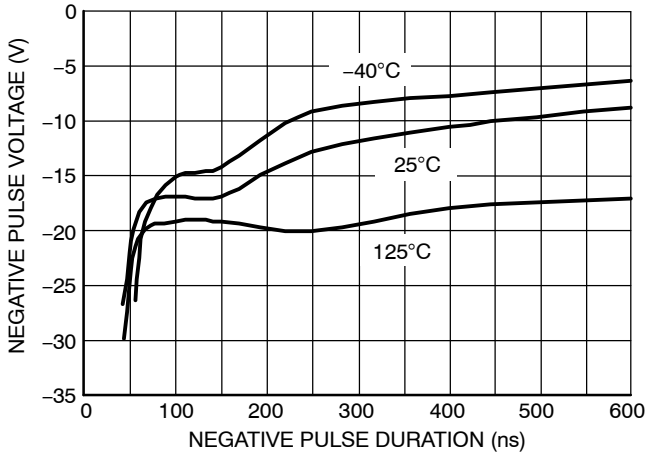


Figure 52. NCP5106B, Negative Voltage Safe Operating Area on the Bridge Pin

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APPLICATION INFORMATION

Negative Voltage Safe Operating Area

When the driver is used in a half bridge configuration, it is possible to see negative voltage appearing on the bridge pin (pin 6) during the power MOSFETs transitions. When the high−side MOSFET is switched off, the body diode of the low−side MOSFET starts to conduct. The negative voltage applied to the bridge pin thus corresponds to the forward voltage of the body diode. However, as pcb copper tracks and wire bonding introduce stray elements (inductance and capacitor), the maximum negative voltage of the bridge pin will combine the forward voltage and the oscillations created by the parasitic elements. As any CMOS device, the deep negative voltage of a selected pin can inject carriers into the substrate, leading to an erratic behavior of the concerned component. ON Semiconductor provides characterization data of its half−bridge driver to show the maximum negative voltage the driver can safely operate with. To prevent the negative injection, it is the designer duty to verify that the amount of negative voltage pertinent to his/her application does not exceed the characterization curve we provide, including some safety margin.

In order to estimate the maximum negative voltage accepted by the driver, this parameter has been characterized over full the temperature range of the component. A test fixture has been developed in which we purposely negatively bias the bridge pin during the freewheel period of a buck converter. When the upper gate voltage shows signs of an erratic behavior, we consider the limit has been reached.

Figure 51 (or 52), illustrates the negative voltage safe operating area. Its interpretation is as follows: assume a negative 10 V pulse featuring a 100 ns width is applied on the bridge pin, the driver will work correctly over the whole die temperature range. Should the pulse swing to −20 V, keeping the same width of 100 ns, the driver will not work properly or will be damaged for temperatures below 125°C.

Summary:

- If the negative pulse characteristic (negative voltage level & pulse width) is above the curves the driver runs in safe operating area.
- If the negative pulse characteristic (negative voltage level & pulse width) is below one or all curves the driver will NOT run in safe operating area.

Note, each curve of the Figure 51 (or 52) represents the negative voltage and width level where the driver starts to fail at the corresponding die temperature.

If in the application the bridge pin is too close of the safe operating limit, it is possible to limit the negative voltage to the bridge pin by inserting one resistor and one diode as follows:

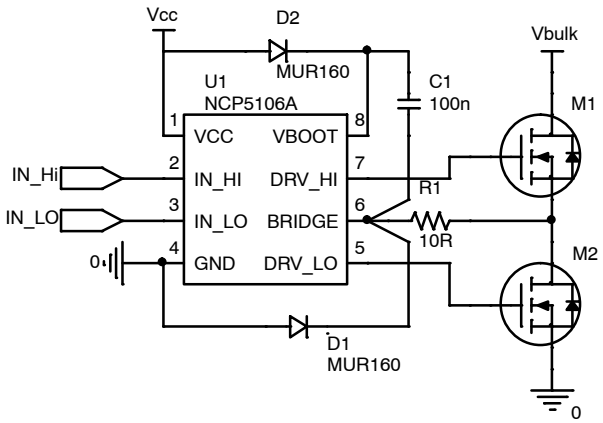


Figure 53. R1 and D1 Improves the Robustness of the Driver

R1 and D1 should be placed as close as possible of the driver. D1 should be connected directly between the bridge pin (pin 6) and the ground pin (pin 4). By this way the negative voltage applied to the bridge pin will be limited by D1 and R1 and will prevent any wrong behavior.

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ORDERING INFORMATION

Device	Package	Shipping†
NCP5106ADR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP5106BDR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel

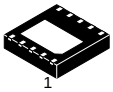
Table 1. DISCONTINUED (Note 6)

Part Number	Package	Temperature Range
NCP5106APG	PDIP−8 (Pb−Free)	50 Units / Rail
NCP5106BPG	PDIP−8 (Pb−Free)	50 Units / Rail
NCP5106AMNTWG	DFN10 (Pb−Free)	4000 / Tape & Reel
NCP5106BMNTWG	DFN10 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

6. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.

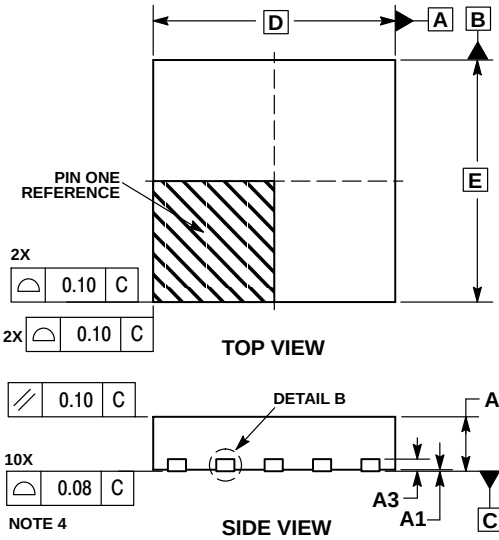
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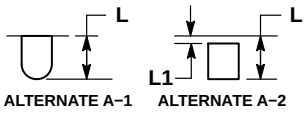


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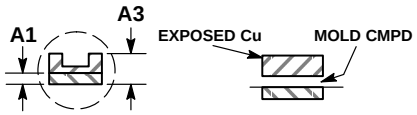
DFN10 4x4, 0.8P
CASE 506DJ
ISSUE O

DATE 20 MAY 2016

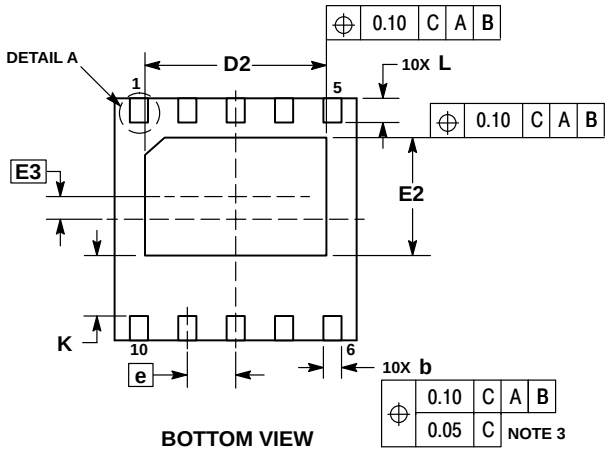




DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS



DETAIL B
ALTERNATE CONSTRUCTIONS



BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. FOR DEVICE OPN CONTAINING W OPTION, DETAIL A ALTERNATE CONSTRUCTION A−2 AND DETAIL B ALTERNATE CONSTRUCTION B−2 ARE NOT APPLICABLE.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	4.00 BSC	
D2	2.90	3.10
E	4.00 BSC	
E2	1.85	2.05
E3	0.375 BSC	
e	0.80 BSC	
K	0.90	−−−
L	0.35	0.45
L1	0.00	0.15

GENERIC MARKING DIAGRAM*

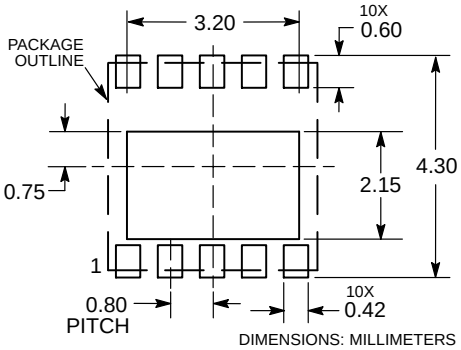


XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

RECOMMENDED MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

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DESCRIPTION:	**DFN10 4X4, 0.8P**	**PAGE 1 OF 1**

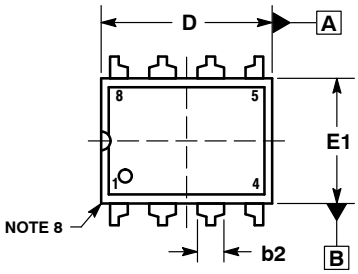
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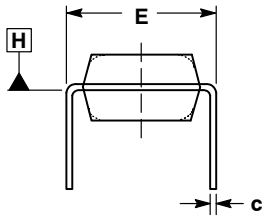
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PDIP–8
CASE 626–05
ISSUE P

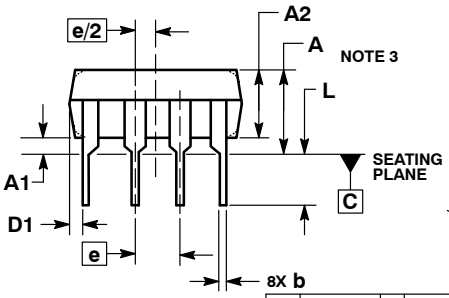
DATE 22 APR 2015



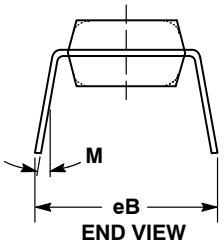
TOP VIEW



END VIEW
WITH LEADS CONSTRAINED
NOTE 5



SIDE VIEW



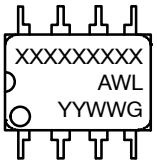
END VIEW
NOTE 6

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS–3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC – IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. V_{CC}

GENERIC
MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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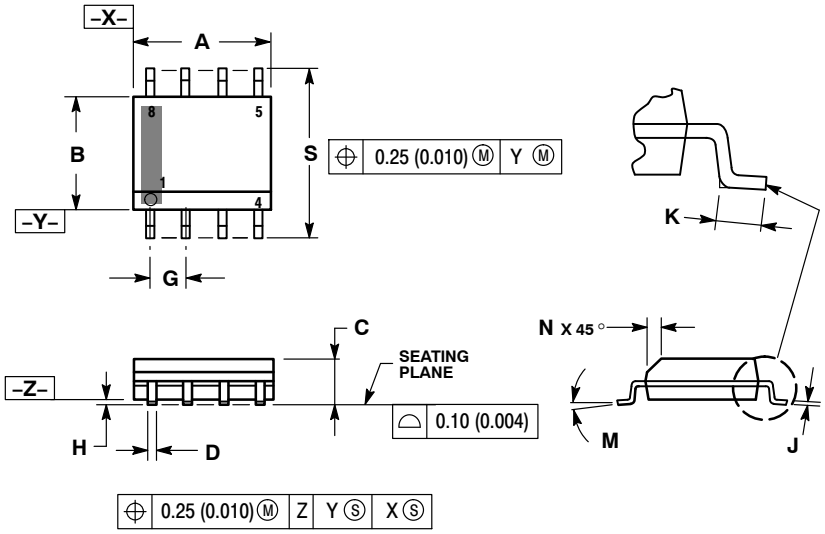
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SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

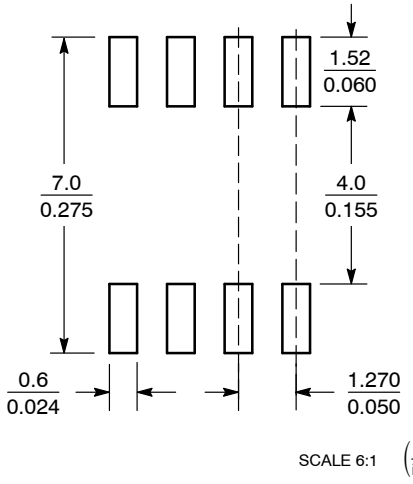
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

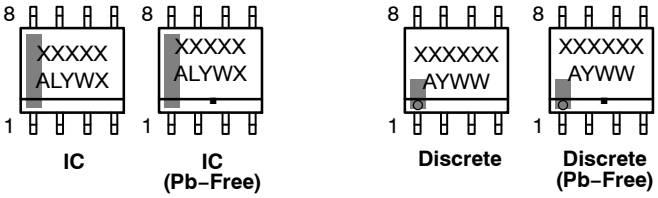
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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