



High Quality Audio J-FET Input Dual Operational Amplifier

■ GENERAL DESCRIPTION

The MUSES8920 is a high quality Audio J-FET input dual operational amplifier. This is a mass production model of MUSES Series. By inheriting MUSES Technology we pursued in the "MUSES series", the MUSES8920 is compatible in high-quality sound and productivity. The MUSES8920 has improved the chip layout and the material, and is developing by thoroughly repeating the listening sound.

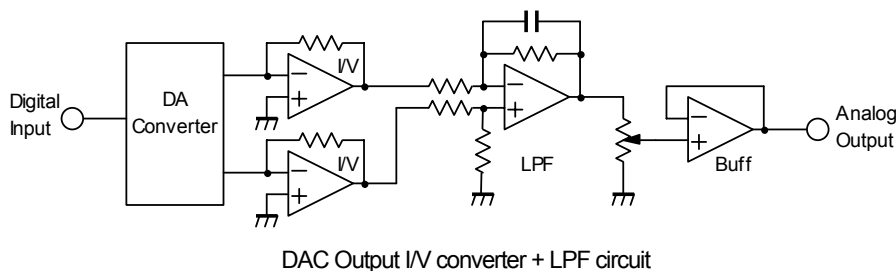
The characteristics Low noise ($8\text{nV}/\sqrt{\text{Hz}}$), high-SR ($25\text{V}/\mu\text{s}$) and low distortion (0.00004% , $A_v=1$) suitable for audio preamplifiers, active filters, and line amplifiers. In addition, taking advantage of the low input bias current that J-FET has, it is suitable for transimpedance amplifier (I/V converter).

■ FEATURES

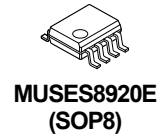
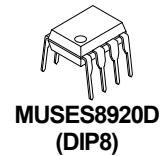
- Operating Voltage $\pm 3.5\text{V}$ to $\pm 16\text{V}$
- Low Noise $8\text{nV}/\sqrt{\text{Hz}}$ typ.
- THD 0.00004% typ. ($A_v=1$)
- Slew Rate $25\text{V}/\mu\text{s}$ typ.
- Channel Separation 150dB typ.
- High Output Current 100mA typ. (short-circuit current)
- Phase Margin 70 deg typ.
- Input Offset Voltage 0.8mV typ. 5mV max.
- Input Bias Current 5pA typ. 250pA max
- Voltage Gain 135dB typ.
- J-FET technology
- Package Outline DIP8, SOP8 JEDEC 150mil

■ APPLICATIONS

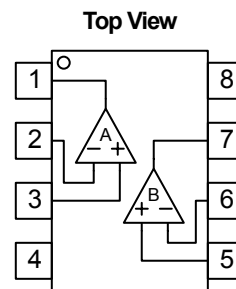
- Current to Voltage (I/V) Converters
- Hi-end Audio
- Active Filters
- Integrators



■ PACKAGE OUTLINE



■ PIN CONFIGURATION



PIN FUNCTION

1. A OUTPUT
2. A -INPUT
3. A +INPUT
4. V-
5. B +INPUT
6. B -INPUT
7. B OUTPUT
8. V+



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MUSES8920

■ ABSOLUTE MAXIMUM RATING (Ta=25°C unless otherwise specified)

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V ⁺ /V	±18	V
Differential Input Voltage Range	V _{ID}	±30(Note1)	V
Common Mode Input Voltage Range	V _{ICM}	±15(Note1)	V
Power Dissipation	P _D	DIP8:870 SOP8:900(Note2)	mW
Operating Temperature Range	T _{opr}	-40~+85	°C
Storage Temperature Range	T _{stg}	-50~+150	°C

(Note1) For supply Voltages less than ±15 V, the maximum input voltage is equal to the Supply Voltage.

(Note2) Mounted on the EIA/JEDEC standard board (114.3×76.2×1.6mm, two layer, FR-4).

(Note3) NJM8920 is ESD (electrostatic discharge) sensitive device.

Therefore, proper ESD precautions are recommended to avoid permanent damage or loss of functionality.

■ RECOMMENDED OPERATING VOLTAGE (Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V ⁺ /V		±3.5	-	±16	V

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS (V⁺/V=±15V, Ta=25°C, V_{cm}=0V unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Current	I _{CC}	R _L =∞, No Signal	-	9	12	mA
Input Offset Voltage	V _{IO}	R _S =50Ω	(-	0.8	mV
Input Bias Current	I _B		(Note4)	-	5	pA
Input Offset Current	I _{IO}		(Note4)	-	2	pA
Voltage Gain1	A _{V1}	R _L =10kΩ, V _o =±13V		106	135	dB
Voltage Gain2	A _{V2}	R _L =2kΩ, V _o =±12.8V		105	133	dB
Voltage Gain3	A _{V3}	R _L =600Ω, V _o =12.5V		105	130	dB
Common Mode Rejection Ratio	CMR	V _{ICM} =±12.5V	(Note5)	80	110	dB
Supply Voltage Rejection Ratio	SVR	V ⁺ /V=±3.5 to ±16V		80	110	dB
Maximum Output Voltage1	V _{OM1}	R _L =10kΩ		±13	±14	V
Maximum Output Voltage2	V _{OM2}	R _L =2kΩ		±12.8	±13.8	V
Maximum Output Voltage3	V _{OM3}	R _L =600Ω		±12.5	±13.5	V
Common Mode Input Voltage Range	V _{ICM}	CMR≥80dB		±12.5	±14	V

(Note4) Written by absolute ratio.

(Note5) CMR is calculated by specified change in offset voltage. (V_{ICM}=0V to +12.5V, V_{ICM}=0V to -12.5V)

● AC CHARACTERISTICS (V⁺/V=±15V, Ta=25°C, V_{cm}=0V unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Gain Bandwidth Product	GB	f=10kHz	-	11	-	MHz
Unity Gain Frequency	f _T	A _V =+100, R _S =100Ω, R _L =2kΩ, C _L =10pF	-	10	-	MHz
Phase Margin	Φ _M	A _V =+100, R _S =100Ω, R _L =2kΩ, C _L =10pF	-	70	-	Deg
Equivalent Input Noise Voltage1	V _{NI1}	f=1kHz	-	8	-	nV/√Hz
Equivalent Input Noise Voltage2	V _{NI2}	RIAA, R _S =2.2kΩ, 30kHz, LPF	-	1.1	3.5	μVrms
Total Harmonic Distortion	THD	f=1kHz, A _V =+10, V _o =5Vrms, R _L =2kΩ	-	0.0004	-	%
Channel Separation	CS	f=1kHz, A _V =-100, R _L =2kΩ	-	150	-	dB
Slew Rate	SR	A _V =1, V _N =2Vp-p, R _L =2kΩ, C _L =10pF	-	25	-	V/μs

■ Application Notes

● Package Power, Power Dissipation and Output Power

IC is heated by own operation and possibly gets damage when the junction power exceeds the acceptable value called Power Dissipation P_D . The dependence of the MUSES8920 P_D on ambient temperature is shown in Fig 1. The plots are depended on following two points. The first is P_D on ambient temperature 25°C, which is the maximum power dissipation. The second is 0W, which means that the IC cannot radiate any more. Conforming the maximum junction temperature T_{jmax} to the storage temperature T_{stg} derives this point. Fig.1 is drawn by connecting those points and conforming the P_D lower than 25°C to it on 25°C. The P_D is shown following formula as a function of the ambient temperature between those points.

$$\text{Dissipation Power } P_D = \frac{T_{jmax} - T_a}{\theta_{ja}} \text{ [W]} \quad (T_a=25^\circ\text{C to } T_a=150^\circ\text{C})$$

Where, θ_{ja} is heat thermal resistance which depends on parameters such as package material, frame material and so on. Therefore, P_D is different in each package.

While, the actual measurement of dissipation power on MUSES8920 is obtained using following equation.

$$(\text{Actual Dissipation Power}) = (\text{Supply Current } I_{cc}) \times (\text{Supply Voltage } V^+ - V^-) - (\text{Output Power } P_o)$$

The MUSES8920 should be operated in lower than P_D of the actual dissipation power.

To sustain the steady state operation, take account of the Dissipation Power and thermal design.

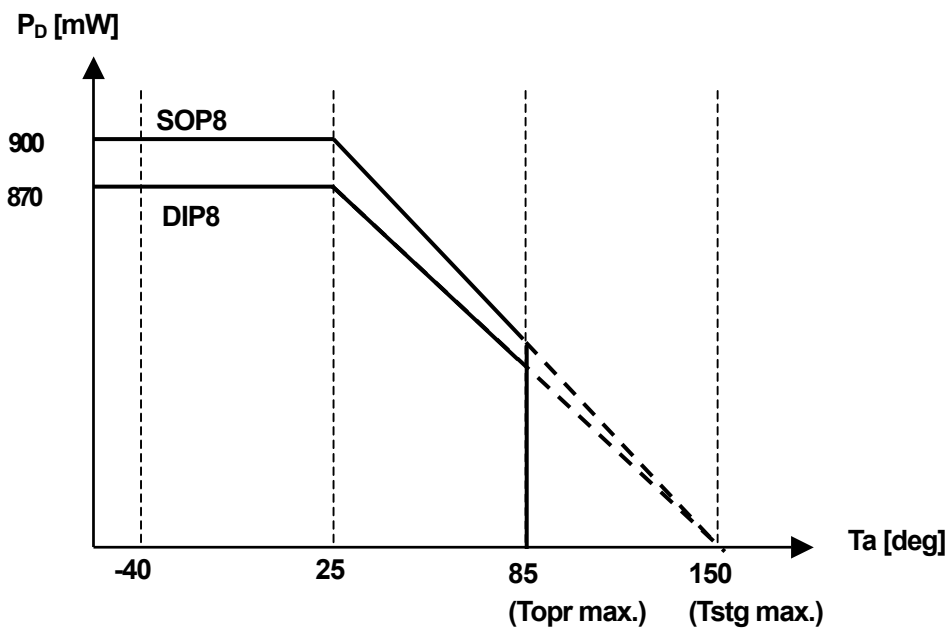
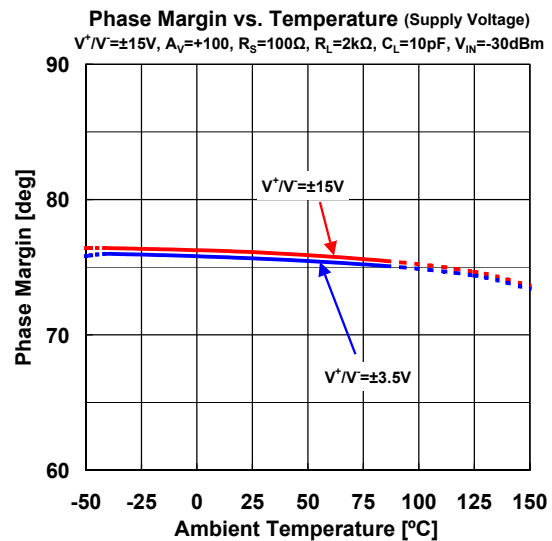
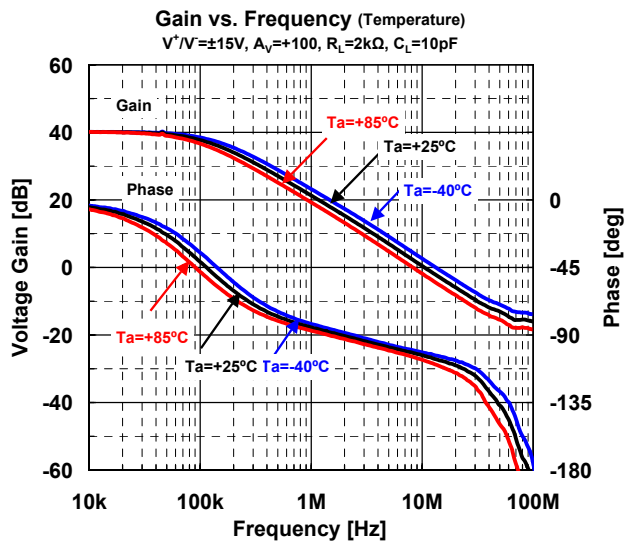
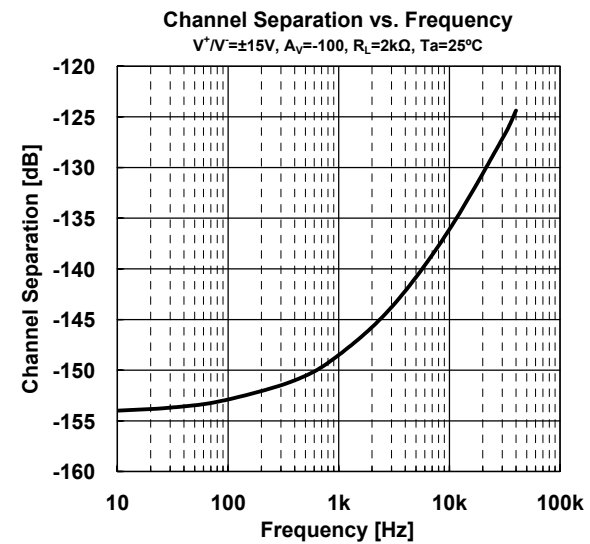
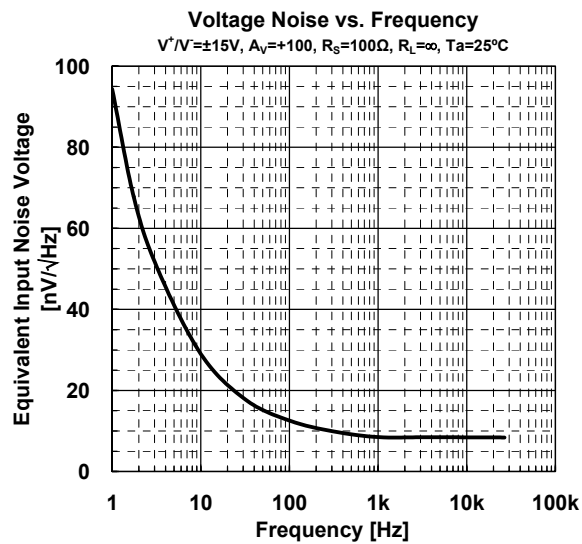
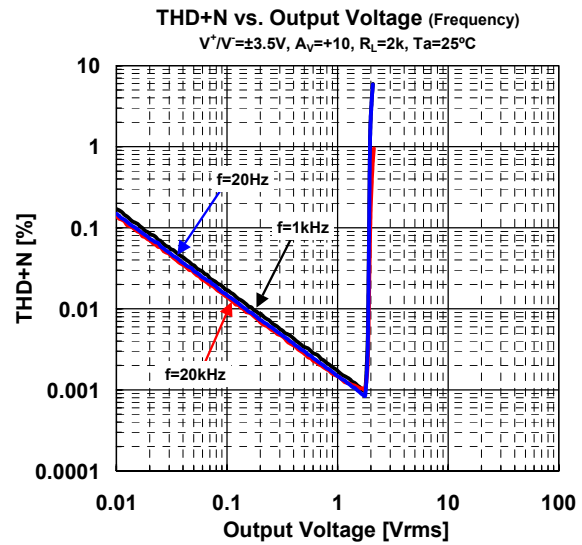
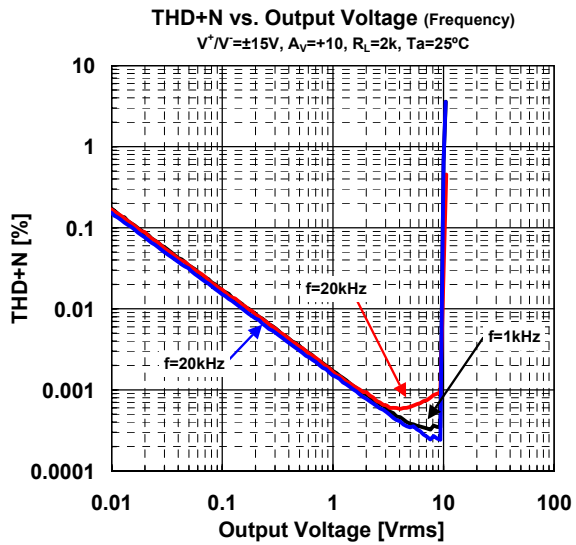


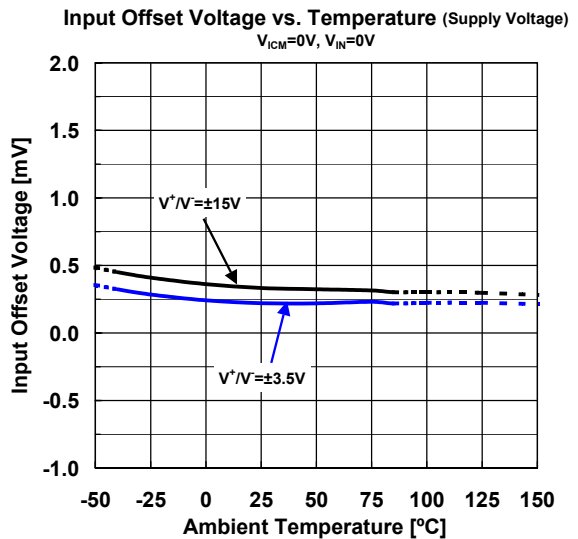
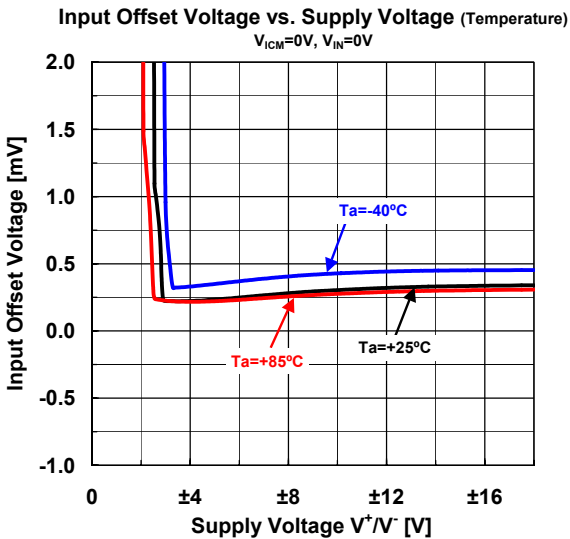
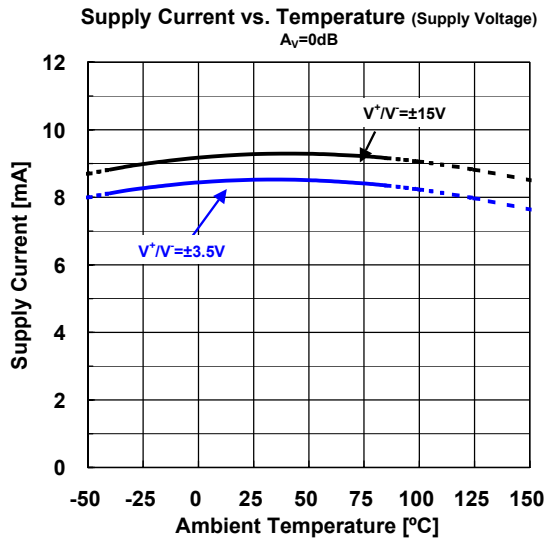
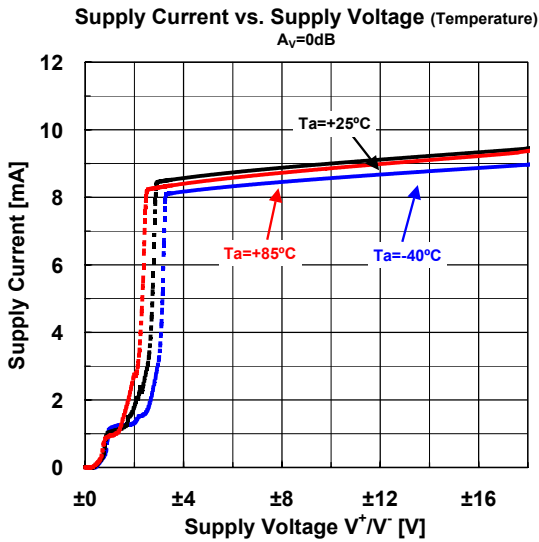
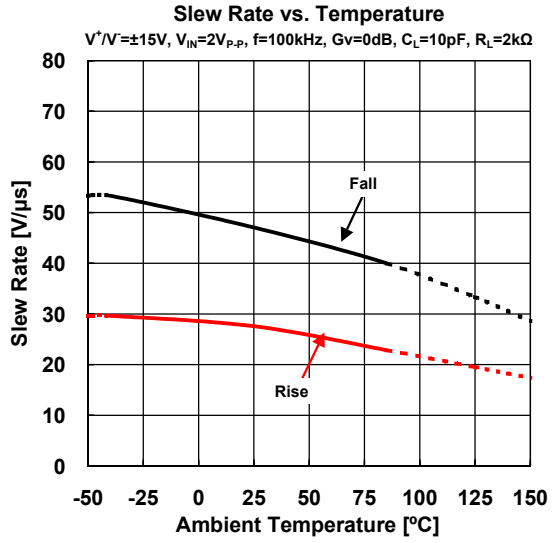
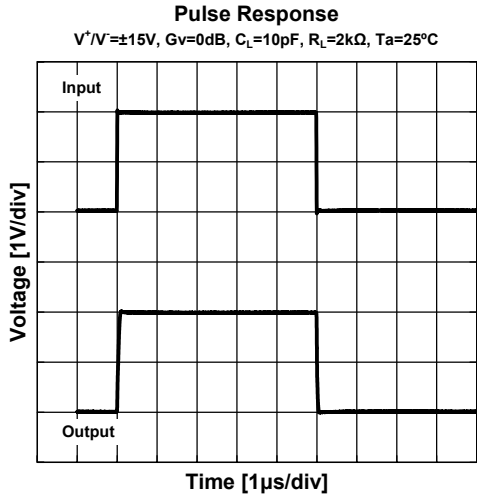
Fig.1 Power Dissipations vs. Ambient Temperature on the MUSES8920

MUSES8920

TYPICAL CHARACTERISTICS



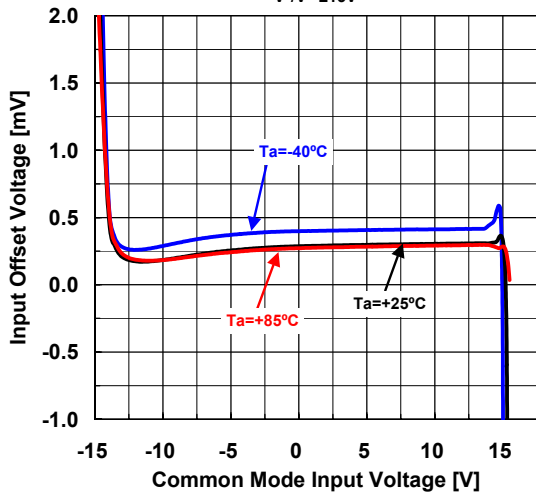
■ TYPICAL CHARACTERISTICS



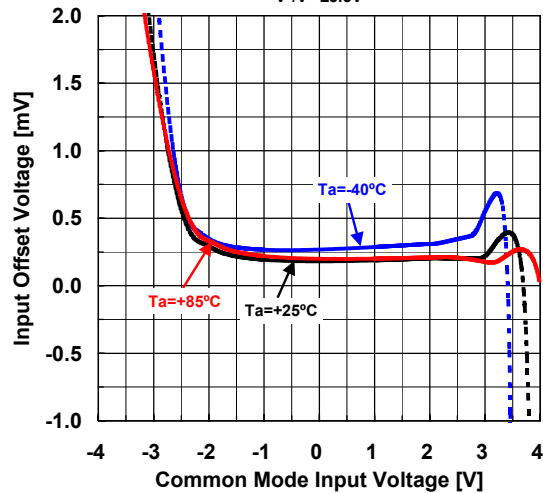
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■ TYPICAL CHARACTERISTICS

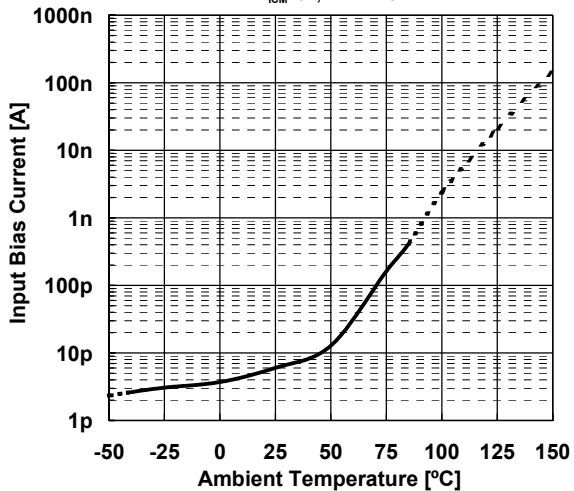
Input Offset Voltage
vs. Common Mode Input Voltage
(Temperature)
 $V^+/V^-=\pm 15V$



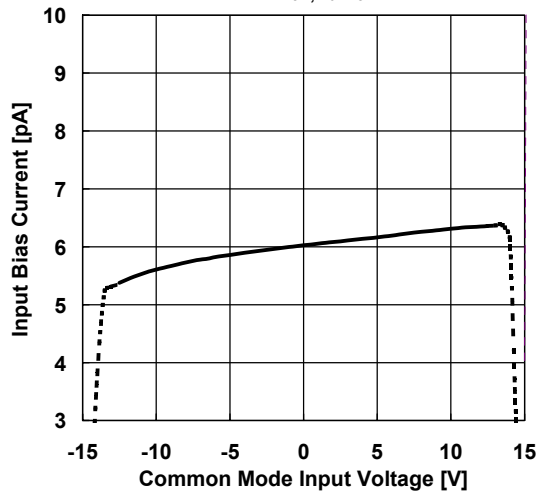
Input Offset Voltage
vs. Common Mode Input Voltage
(Temperature)
 $V^+/V^-=\pm 3.5V$



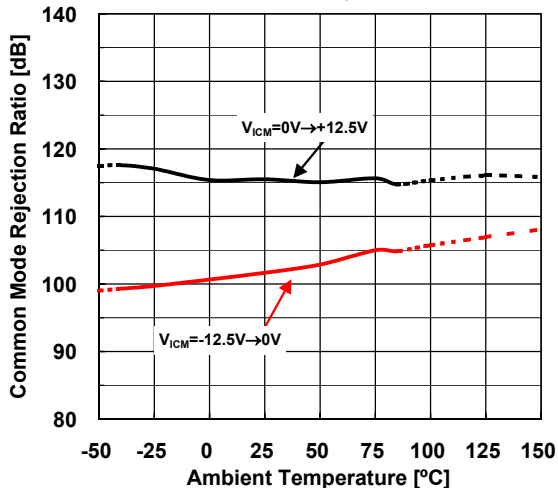
Input Bias Current vs. Temperature (Supply Voltage)
 $V_{ICM}=0V, V^+/V^-=\pm 15V$



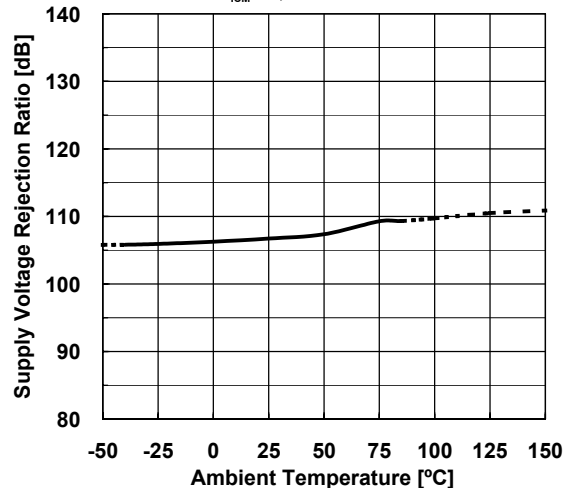
Input Bias Current vs. Common Mode Input Voltage
(Temperature)
 $V^+/V^-=\pm 15V, T_a=25^\circ C$



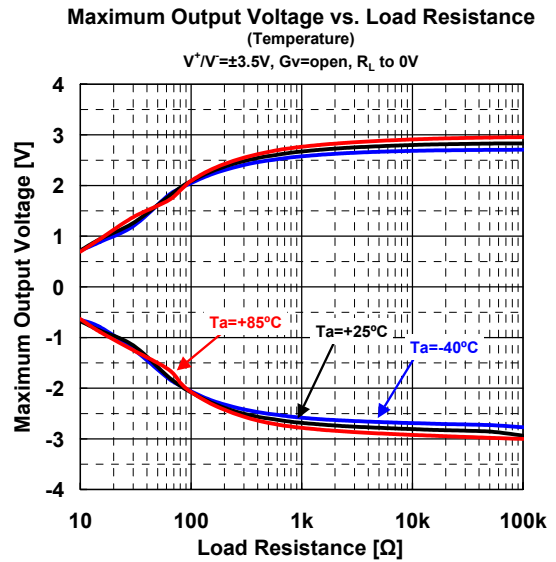
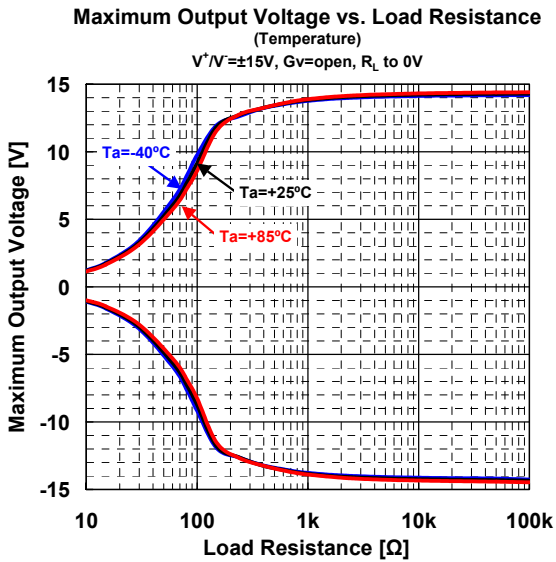
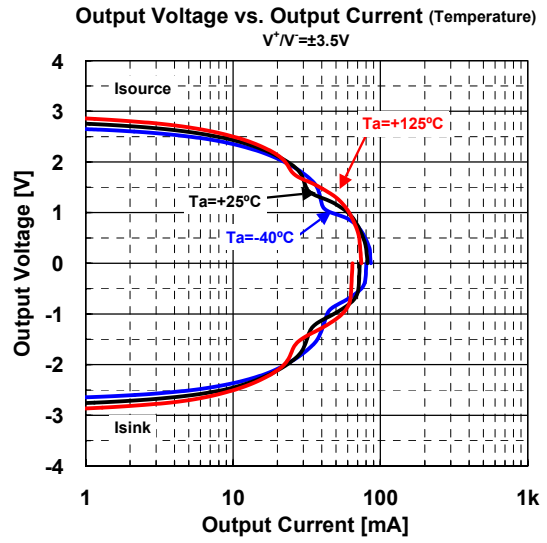
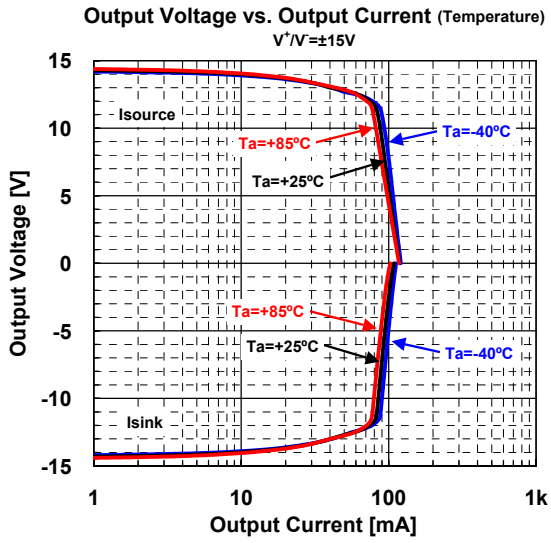
CMR vs. Temperature
 $V^+/V^-=\pm 15V$



SVR vs. Temperature
 $V_{ICM}=0V, V^+/V^-=\pm 3.5V \rightarrow \pm 16V$

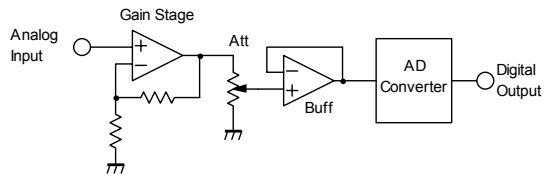


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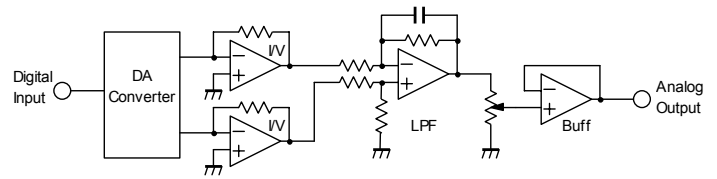


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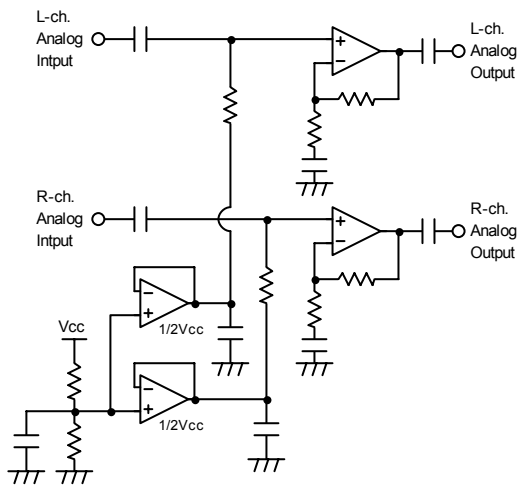
APPLICATION CIRCUIT



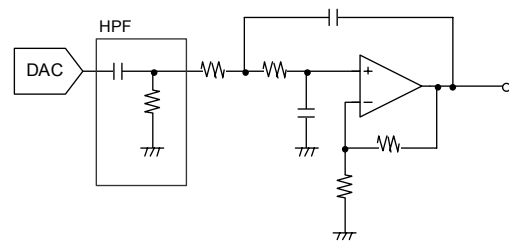
(Fig.1: ADC Input)



(Fig.2: DAC Output)



(Fig.3: Half Vcc Buffer on Single Supply Application)



(Fig.4: DAC LPF Circuit)

<CAUTION>
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