

**DESCRIPTION**

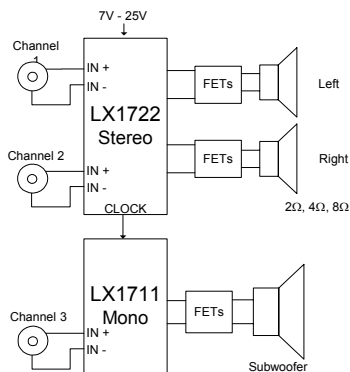
The LX1721/1722 is a monolithic high performance Class-D stereo controller IC designed for high efficiency or space constrained audio requirements such as portable or battery operated products, automotive amplifiers, and multi-channel multimedia computer and video game applications. This high frequency, full audio bandwidth switching power amplifier controller offers dramatically improved performance over Linfinity's previous generation amplifier products. Enhancements include higher output power, better SNR, lower noise floor, and reduced THD. Combined with output power MOSFET's and an output filter, the LX1721/1722 is a complete Class-D audio solution.

A complete audio amplifier module is available to quickly evaluate the LX1721 or LX1722 stereo controller. Simply connect the amplifier to the power source, audio signal, and speakers. Reference designs support a variety of requirements including multi channel systems, subwoofers, satellite / subwoofer combinations and various speaker loads (2Ω, 4Ω, 8Ω). The versatile amplifier solution can easily be adjusted for frequency response, optimized for efficiency and performance, or designed to minimize PCB area and component count. The LX1721/1722 is available in a space saving 44-pin QSOP package. (Continued Next Page)

**IMPORTANT:** For the most current data, consult MICROSEMI's website: <http://www.microsemi.com>

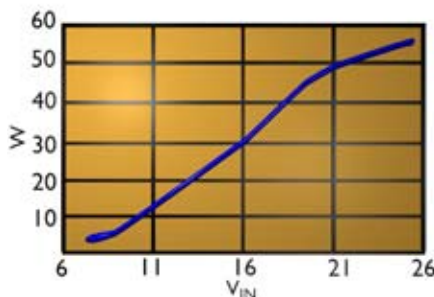
**KEY FEATURES**

- Integrated Switching Class-D Stereo Controller IC
- Full 20Hz-20kHz Audio Bandwidth
- High Fidelity (LX1721) Or High Power (LX1722) Versions Available
- Single Supply Operation
- THD+N <0.06% Typical (1Wrms, 1kHz, 4Ω)
- Maximum Efficiency 80%-85%
- Output Power >60Wrms per Channel (LX1722, 4Ω, 1% THD+N)
- PSRR -70dB Typical
- Differential Input To Minimize Noise Effects
- Supports Multi-Channel Systems
- Complete LX1721 or LX1722 Amplifier Evaluation Module Available
- 44-Pin QSOP Package

**PRODUCT HIGHLIGHT**


**2.1 Audio Amplifier Configuration**

**Output Power vs. Supply Voltage**  
1kHz, 4Ω, THD+N=1%


**APPLICATIONS**

- Multimedia Speakers
- Surround Sound Game Systems
- Notebook Computers
- Desktop Computers
- Automotive Amplifiers And Head units
- Battery Operated Equipment (Megaphone, Public Address System)
- Portable Audio (Boom Box)
- Wireless Speakers
- High Power Subwoofer
- Automotive Audio Systems
- Home Theatre

**PACKAGE ORDER INFO**

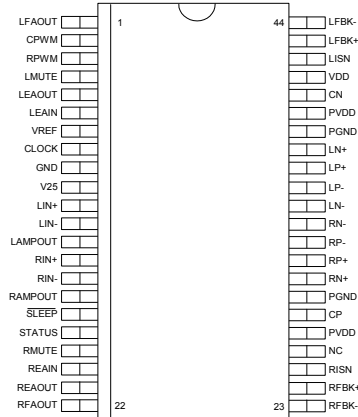
| T <sub>J</sub> (°C) | V <sub>DD</sub> | DB | Plastic QSOP 44-Pin |
|---------------------|-----------------|----|---------------------|
| -20 to 70           | 7V – 15V        |    | LX1721CDB           |
| -20 to 70           | 7V – 25V        |    | LX1722CDB           |

Note: Available in Tape & Reel.  
Append the letter "T" to the part number. (i.e. LX1722CDBT)

**THERMAL DATA**
**DB**
**44-PIN QSSOP PACKAGE**
**THERMAL RESISTANCE-JUNCTION TO AMBIENT,  $\theta_{JA}$** 
**50°C/W**

 Junction Temperature Calculation:  $T_J = T_A + (P_D \times \theta_{JA})$ .

 The  $\theta_{JA}$  numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

**PACKAGE PIN OUT**

**DB PACKAGE**  
 (Top View)

**DESCRIPTION (CONTINUED)**

The stereo output controller is available in either an LX1722 high power version (>65Wrms, 4Ω) with a supply voltage range of 7V-25V or an LX1721 high fidelity version (better SNR performance) with a supply voltage range of 7V-15V. The current rating of the external MOSFET's, the available supply voltage, and speaker load primarily limits the maximum output power. The amplifier provides high fidelity performance and is designed to operate over the full 20Hz to 20kHz audio band. Signal distortion measurements yield.

THD+N levels of 0.06%(1kHz, 1Wrms). Efficiency is greater than 80% typical, which eliminates the need for heatsinks in most applications. The AudioMAX™ solution requires a single supply voltage, simplifying input power requirements where a dual supply may not be available. To minimize potential environmental noise issues and ease the integration of the amplifier into a variety of applications, features such as a balanced/differential audio input and a high power supply rejection ratio help reduce the effects of noise from the audio signal or power supply.

**FUNCTIONAL PIN DESCRIPTION**

| PIN NAME       | DESCRIPTION                              | PIN NAME     | DESCRIPTION                                     |
|----------------|------------------------------------------|--------------|-------------------------------------------------|
| <b>LFAOUT</b>  | Left Feedback Amplifier Output           | <b>LFBK-</b> | Left Feedback Amplifier Inverting Input         |
| <b>CPWM</b>    | PWM Capacitor Connection                 | <b>LFBK+</b> | Left Feedback Amplifier Non-Inverting Input     |
| <b>RPWM</b>    | PWM Resistor Connection                  | <b>LISN</b>  | Left Current Limit Sense Input                  |
| <b>LMUTE</b>   | Left Mute Input (Active High)            | <b>VDD</b>   | Analog Supply Voltage                           |
| <b>LEAOUT</b>  | Left Error Amplifier Output              | <b>CN</b>    | Supply Decoupling for NFET Drivers              |
| <b>LEAIN</b>   | Left Inverting Input of Error Amplifier  | <b>PVDD</b>  | Output Driver Supply Voltage                    |
| <b>VREF</b>    | 5V Reference                             | <b>PGND</b>  | Output Driver High Current Ground               |
| <b>CLOCK</b>   | Input / Output Clock for Synch Operation | <b>LN+</b>   | Left Drive for NFET on Positive Half of Bridge  |
| <b>GND</b>     | Low Current Ground                       | <b>LP+</b>   | Left Drive for PFET on Positive Half of Bridge  |
| <b>V25</b>     | 2.5V Reference                           | <b>LP-</b>   | Left Drive for PFET on Negative Half of Bridge  |
| <b>LIN+</b>    | Left Positive Audio Input                | <b>LN-</b>   | Left Drive for NFET on Negative Half of Bridge  |
| <b>LIN-</b>    | Left Negative Audio Input                | <b>RN-</b>   | Right Drive for NFET on Negative Half of Bridge |
| <b>LAMPOUT</b> | Left Input Amplifier Output              | <b>RP-</b>   | Right Drive for PFET on Negative Half of Bridge |
| <b>RIN+</b>    | Right Positive Audio Input               | <b>RP+</b>   | Right Drive for PFET on Positive Half of Bridge |
| <b>RIN-</b>    | Right Negative Audio Input               | <b>RN+</b>   | Right Drive for NFET on Positive Half of Bridge |
| <b>RAMPOUT</b> | Right Input Amplifier Output             | <b>PGND</b>  | Output Driver High Current Ground               |
| <b>SLEEP</b>   | Sleep Input (active low)                 | <b>CP</b>    | Supply Decoupling for PFET Drivers              |
| <b>STATUS</b>  | UVLO Indicator (Open Collector Output)   | <b>PVDD</b>  | Output Driver Supply Voltage                    |
| <b>RMUTE</b>   | Right Mute Input (Active High)           | <b>NC</b>    | No Connect                                      |
| <b>REAIN</b>   | Right Inverting Input of Error Amplifier | <b>RISN</b>  | Right Current Limit Sense Input                 |
| <b>REAOUT</b>  | Right Error Amplifier Output             | <b>RFBK+</b> | Left Feedback Amplifier Non-Inverting Input     |
| <b>RFAOUT</b>  | Right Feedback Amplifier Output          | <b>RFBK-</b> | Right Feedback Amplifier Inverting Input        |

**ABSOLUTE MAXIMUM RATINGS**

|                                          |                          |
|------------------------------------------|--------------------------|
| Supply Voltage (PVDD, VDD)               | -0.3V to 30V             |
| SLEEP, STATUS, R/LFBK+, R/LFBK-          | -0.3V to VDD +0.3V       |
| R/LISN                                   | PVDD -2 to PVDD to +0.3V |
| RPWM, CPWM, R/LMUTE                      | -0.3V to VREF +0.3V      |
| R/LIN+, R/LIN-, R/LAMPOUT                | -0.3V to VREF +0.3V      |
| R/LEAIN, R/LEAOUT, R/LFAOUT              | -0.3V to VREF +0.3V      |
| CLOCK                                    | -0.3V to CN +0.3V        |
| Operating Junction Temperature Plastic   | 125°C                    |
| Storage Temperature Range                | -65°C to 150°C           |
| Lead Temperature (Soldering, 10 seconds) | 300°C                    |

Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into negative out of the specified terminal.

**ELECTRICAL CHARACTERISTICS**

Unless otherwise specified, the following specifications apply over the operating ambient temperature  $-20^{\circ}\text{C} < T_A < 70^{\circ}\text{C}$  (NOTE 2).

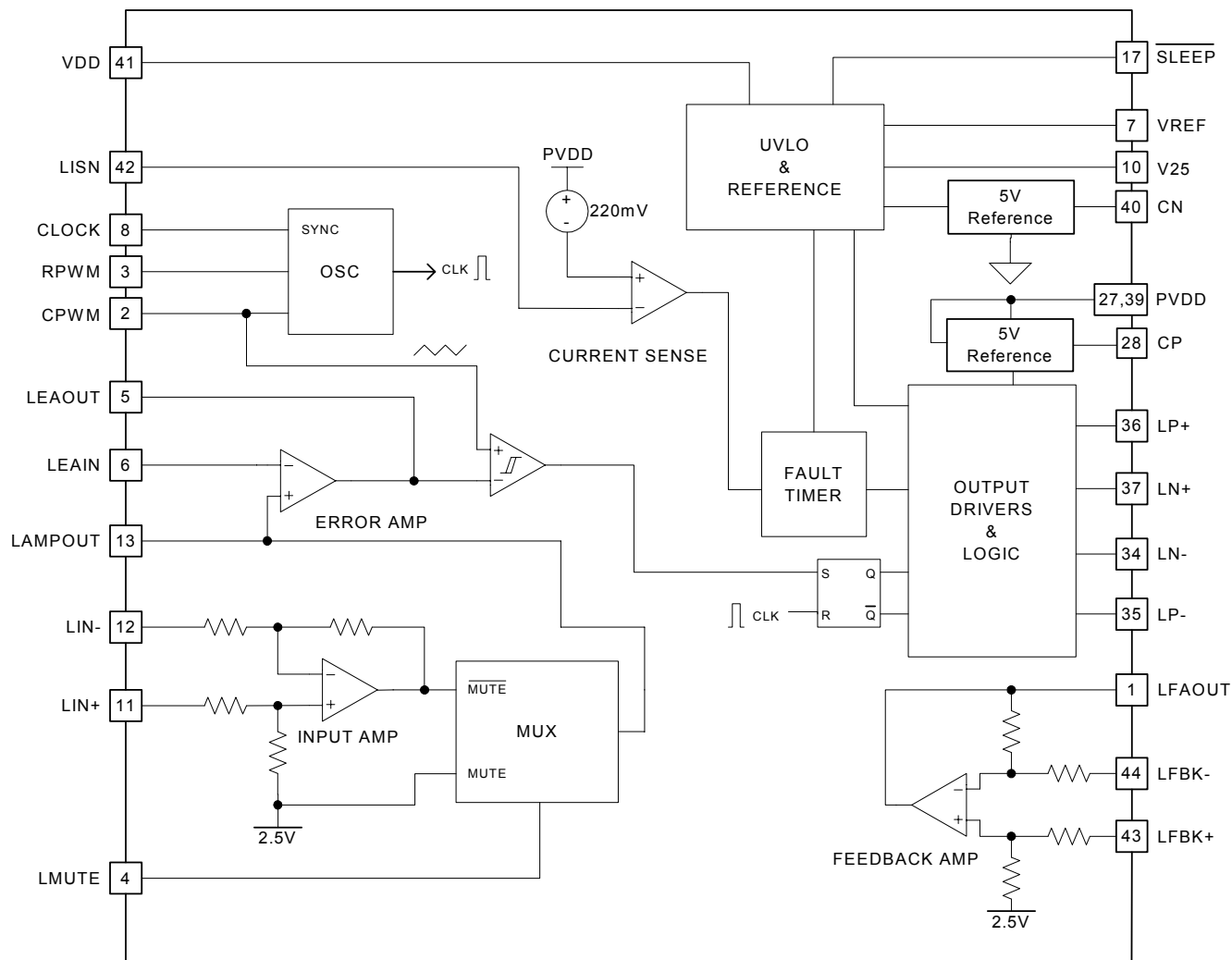
Test conditions: RPWM = 34.8k, CPWM = 100pF, VDD = PVDD = 15V

| Parameter                            | Symbol           | Test Conditions                                                                 | LX1721 / 1722 |      |       | Units |
|--------------------------------------|------------------|---------------------------------------------------------------------------------|---------------|------|-------|-------|
|                                      |                  |                                                                                 | Min           | Typ  | Max   |       |
| Evaluation Module (See LX1721)       |                  |                                                                                 |               |      |       |       |
| Supply Voltage                       | LX1721           | V <sub>DD</sub>                                                                 | 7             |      | 15    | V     |
|                                      | LX1722           |                                                                                 | 7             |      | 25    |       |
| Power Supply Rejection Ratio         | PSRR             | V <sub>IN</sub> = 15V, V <sub>RIIPPLE</sub> = 1V <sub>RMS</sub> , 20Hz to 20kHz |               | -70  |       | dB    |
| Output Power (Per Channel)           | P <sub>O</sub>   | V <sub>IN</sub> = 15V, R <sub>L</sub> =4Ω, THD+N=1%, 10Hz to 22kHz              |               | 25   |       | W     |
|                                      |                  | V <sub>IN</sub> = 25V, R <sub>L</sub> =4Ω, THD+N=1%, 10Hz to 22kHz              |               | 60   |       |       |
| Efficiency                           |                  | V <sub>IN</sub> = 15V, f <sub>IN</sub> = 1kHz, P <sub>O</sub> = 10W             |               | 82   |       | %     |
|                                      |                  | V <sub>IN</sub> = 15V, f <sub>IN</sub> = 1kHz, P <sub>O</sub> = 20W             |               | 85   |       |       |
| Total Harmonic Distortion Plus Noise | THD+N            | f <sub>IN</sub> = 1kHz, P <sub>O</sub> = 1W                                     |               | .06  |       | %     |
|                                      |                  | f <sub>IN</sub> = 20Hz to 20kHz, P <sub>O</sub> = 1W                            |               |      | .2    |       |
| Signal-To-Noise Ratio                | SNR              | R <sub>L</sub> = 4Ω, P <sub>O</sub> = 1W                                        |               | 81   |       | dBr   |
| Oscillator Section                   |                  |                                                                                 |               |      |       |       |
| Oscillator Frequency                 | F <sub>OSC</sub> |                                                                                 |               | 450  |       | kHz   |
| Charge Current                       | I <sub>CHG</sub> | (varies with V <sub>DD</sub> pin voltage)                                       |               | -225 |       | μA    |
| Discharge Current                    | I <sub>DIS</sub> | (varies with V <sub>DD</sub> pin voltage)                                       |               | 225  |       | μA    |
| Oscillator Peak Voltage              | V <sub>PK</sub>  | (varies with V <sub>DD</sub> pin voltage)                                       |               | 3.6  |       | V     |
| Oscillator Valley Voltage            | V <sub>VAL</sub> | (varies with V <sub>DD</sub> pin voltage)                                       |               | 1.4  |       | V     |
| Voltage Stability                    |                  | V <sub>DD</sub> = 8V to 25V                                                     |               | 0.6  | 2     | %     |
| Temperature Stability                |                  | T <sub>A</sub> = 0°C to 70°C                                                    |               | 1.0  | 2     | %     |
| Error Amplifier                      |                  |                                                                                 |               |      |       |       |
| Input Offset Voltage                 | V <sub>IO</sub>  |                                                                                 |               | 5    |       | mV    |
| DC Open Loop Gain                    | A <sub>OL</sub>  |                                                                                 |               | 60   |       | dB    |
| Unity Gain Bandwidth                 | UGBW             |                                                                                 |               | 7    |       | MHz   |
| High Output Voltage                  | V <sub>OH</sub>  | I <sub>OUT</sub> = -100μA                                                       | 3.5           |      |       | V     |
| Low Output Voltage                   | V <sub>OL</sub>  | I <sub>OUT</sub> = +100μA                                                       |               |      | 100   | mV    |
| Input Bias Current                   | I <sub>IN</sub>  | V <sub>IN</sub> = 1V to 4V                                                      |               | 1    |       | μA    |
| Input Amplifier                      |                  |                                                                                 |               |      |       |       |
| Stage Gain                           |                  | Set by Internal Resistors                                                       | 3.465         | 3.5  | 3.535 | V/V   |
| Output Voltage, High                 | V <sub>OH</sub>  | I <sub>OUT</sub> = -100μA                                                       | 3.85          |      |       | V     |
| Output Voltage, Low                  | V <sub>OL</sub>  | I <sub>OUT</sub> = +100μA                                                       |               |      | 1.3   | V     |
| Input Impedance                      |                  |                                                                                 |               | 180  |       | kΩ    |
| Feedback Amplifier                   |                  |                                                                                 |               |      |       |       |
| Stage Gain                           | LX1721           | Set by Internal Resistors                                                       | 89            | 91   | 93    | mV/V  |
|                                      | LX1722           | Set by Internal Resistors                                                       | 56            | 57   | 58    | mV/V  |
| Input Impedance                      | LX1721           |                                                                                 |               | 250  |       | kΩ    |
|                                      | LX1722           |                                                                                 |               | 400  |       | kΩ    |

**ELECTRICAL CHARACTERISTICS (CONTINUED)**

| Parameter                                                          | Symbol          | Test Conditions                                                         | LX1721 / 1722 |        |       | Units  |
|--------------------------------------------------------------------|-----------------|-------------------------------------------------------------------------|---------------|--------|-------|--------|
|                                                                    |                 |                                                                         | Min           | Typ    | Max   |        |
| Current Limit Comparator                                           |                 |                                                                         |               |        |       |        |
| Voltage Sense Threshold                                            |                 |                                                                         | 190           | 210    | 230   | mV     |
| Blanking Pulse Delay                                               |                 |                                                                         |               | 500    |       | ns     |
| Response Time                                                      |                 | Excluding blanking pulse                                                |               | 250    |       | ns     |
| I <sub>UM</sub> Pulses required to Current Limit Latch             |                 |                                                                         | 4             | 4      | 4     | cycles |
| Consecutive Clear Pulses required to reset I <sub>UM</sub> counter |                 |                                                                         | 2             | 2      | 2     | cycles |
| Reference Voltage Section                                          |                 |                                                                         |               |        |       |        |
| Initial Accuracy (VREF)                                            |                 |                                                                         |               | 5.0    |       |        |
| Voltage Stability (VREF)                                           |                 |                                                                         |               | ± 50   | ± 100 | mV     |
| Initial Accuracy (V25)                                             |                 |                                                                         |               | 2.5    |       |        |
| Voltage Stability (V25)                                            |                 |                                                                         |               | ± 25   | ± 50  | mV     |
| Temperature Stability                                              |                 | T <sub>A</sub> = 0°C to 70°C                                            |               | 2      | 5     | mV     |
| Line Regulation                                                    |                 | V <sub>DD</sub> = 9V to 15V                                             |               | 0.5    |       | mV     |
| Load Regulation                                                    |                 | I <sub>OUT</sub> = 0 to 10mA                                            |               | 5      |       | mV     |
| Under Voltage Lockout Section                                      |                 |                                                                         |               |        |       |        |
| Start Threshold Voltage                                            |                 |                                                                         |               | 6      |       | V      |
| UV Lockout Hysteresis                                              |                 |                                                                         |               | 250    |       | mV     |
| UVLO Delay To Output Enable                                        |                 |                                                                         |               | 62,500 |       | clkcy  |
| Supply Current                                                     |                 |                                                                         |               |        |       |        |
| Sleep Current                                                      |                 | SLEEP Input = 0V, T <sub>A</sub> = 25°C                                 |               | 30     |       | μA     |
| Operating Current                                                  |                 | SLEEP Input = 2V, V <sub>IN</sub> = 15V, No MOSFETs connected           |               | 8      | 11    | mA     |
| Sleep to Output Enable                                             |                 |                                                                         |               | 62,500 |       | clkcy  |
| Sleep Threshold                                                    |                 |                                                                         | 1.45          | 1.6    | 1.75  | V      |
| Mute Section                                                       |                 |                                                                         |               |        |       |        |
| Mute Threshold                                                     |                 |                                                                         | 1.2           | 1.35   | 1.5   | V      |
| Output Drivers For N-Channel MOSFETs                               |                 |                                                                         |               |        |       |        |
| NFET Drivers, Low Level Voltage                                    | V <sub>OL</sub> | I <sub>SINK</sub> = 3mA                                                 |               | 30     | 100   | mV     |
|                                                                    |                 | I <sub>SINK</sub> = 100mA                                               |               | 0.3    | 1.0   | V      |
| NFET Drivers, High Level Voltage                                   | V <sub>OH</sub> | I <sub>SOURCE</sub> = 3mA, C <sub>N</sub> = 5.2V applied externally     |               | 30     | 100   | mV     |
|                                                                    |                 | I <sub>SOURCE</sub> = 100mA, C <sub>N</sub> = 5.2V applied externally   |               | 0.3    | 1.0   | V      |
| Output Drives For P-Channel MOSFETs                                |                 |                                                                         |               |        |       |        |
| PFET Drivers, Low Level Voltage                                    | V <sub>OL</sub> | I <sub>SINK</sub> = 3mA                                                 |               | 30     | 100   | mV     |
|                                                                    |                 | I <sub>SINK</sub> = 100mA                                               |               | 0.5    | 1.0   | V      |
| PFET Drivers, High Level Voltage                                   | V <sub>OH</sub> | I <sub>SOURCE</sub> = 3mA, C <sub>P</sub> = 5.2V (applied externally)   |               | 30     | 100   | mV     |
|                                                                    |                 | I <sub>SOURCE</sub> = 100mA, C <sub>P</sub> = 5.2V (applied externally) |               | 0.5    | 1.0   | V      |

Note 2: The LX1721 / 22CDB is guaranteed to meet performance specifications from 0° to 70°C. Specifications over the -20° to 0°C operation temperature range are assured by design, characterization, and statistical process control.

**BLOCK DIAGRAM**


**FIGURE 1 – LX1721 / 22 SIMPLIFIED BLOCK DIAGRAM (LEFT CHANNEL CIRCUIT SHOWN)**

**APPLICATION INFORMATION**
**Frequency Synchronization**

Two or more LX1721 / LX1722 oscillators can be configured for synchronous operation. One unit, the master, is programmed for the desired frequency with the  $R_{PWM}$  and  $C_{PWM}$  as usual. Additional units will be slave units, and their oscillators will be disabled by leaving the  $R_{PWM}$  pin disconnected. The CLOCK pin and the  $C_{PWM}$  pin of the slave units should be tied to the CLOCK pin and the  $C_{PWM}$  pin of the master unit respectively. In this configuration, the CLOCK pins of the slave units begin receiving instead of transmitting clock pulses. Also, the  $C_{PWM}$  pins quit driving the PWM capacitor in the slave units. Note that for optimum performance, all slave units should be located within a few inches of the master unit.

**Oscillator Configuration ( $R_{PWM}$  and  $C_{PWM}$  selection)**

The oscillator is programmed by the external timing components  $R_{PWM}$  and  $C_{PWM}$ . For a nominal frequency of 333kHz,  $R_{PWM}$  and  $C_{PWM}$  should be set to 49.9kOhms and 100pF respectively. Note that in order to keep the slope of the PWM ramp voltage proportional to the supply voltage, both the ramp peak and valley voltages, and the charge and discharge currents are proportional to the supply voltage. This keeps the frequency relatively constant while keeping the slope of the PWM ramp proportional to the voltage on the VDD pin. For operating frequencies other than 333kHz, the frequency can be approximated by the following equation:

$$\text{Frequency} = \frac{1}{(0.577)(R_{PWM})(C_{PWM}) + 320ns}$$



#### CHARACTERISTIC CURVES

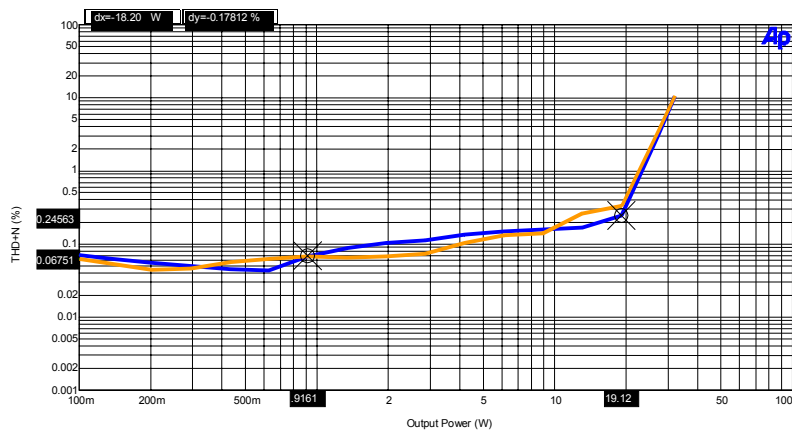


FIGURE 2 – THD+N VS. OUTPUT POWER

$V_{IN} = 15V$   
 $f_{IN} = 1kHz$   
 $R_L = 4\Omega$

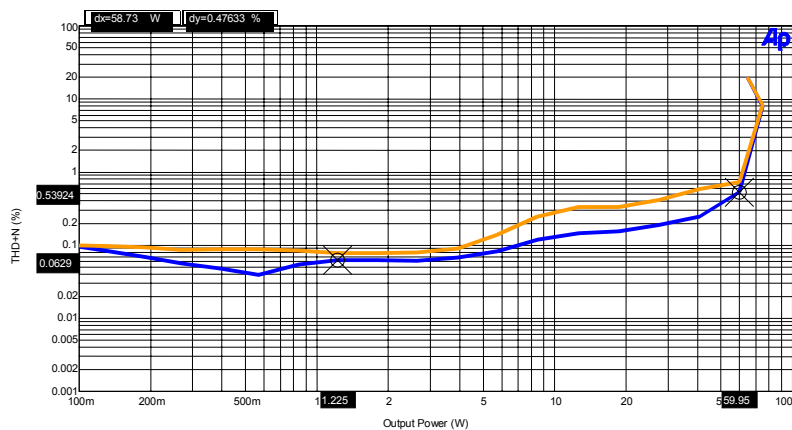


FIGURE 3 – THD+N VS. OUTPUT POWER

$V_{IN} = 25V$   
 $f_{IN} = 1kHz$   
 $R_L = 4\Omega$

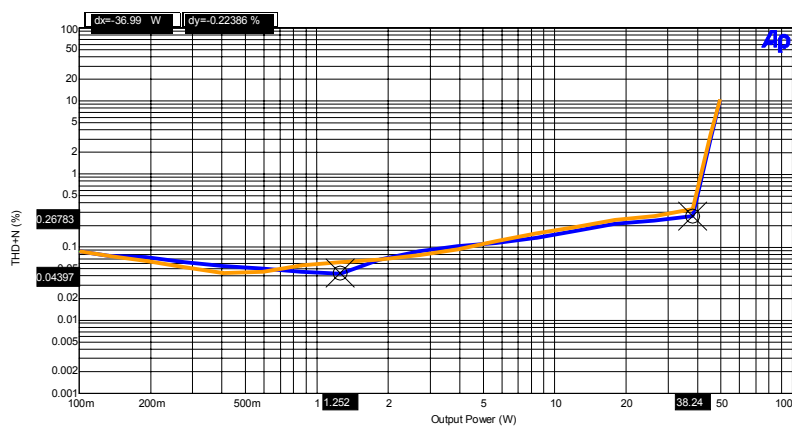
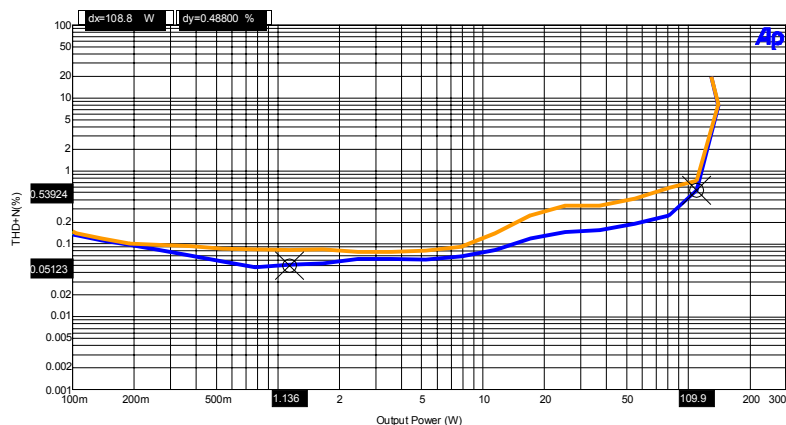
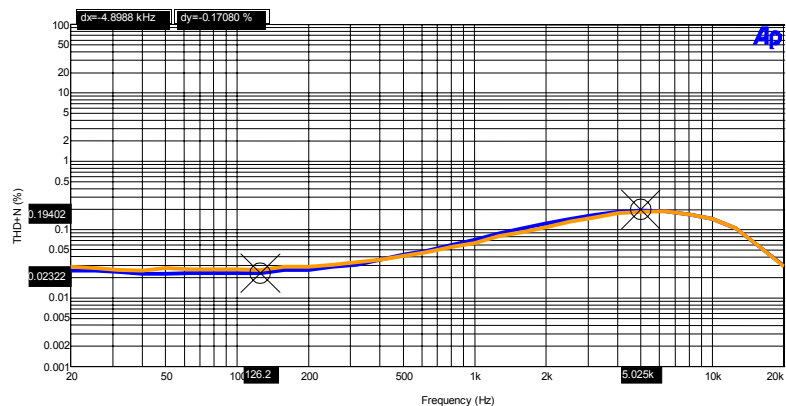


FIGURE 4 – THD+N VS. OUTPUT POWER

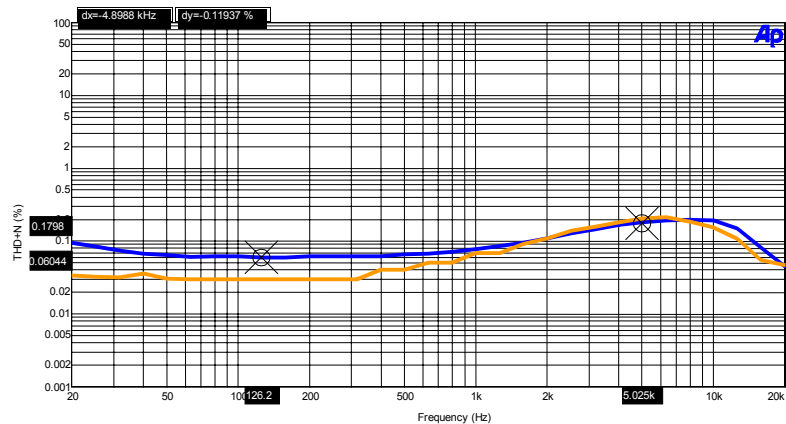
$V_{IN} = 15V$   
 $f_{IN} = 1kHz$   
 $R_L = 2\Omega$

**CHARACTERISTIC CURVES (CONTINUED)**

**FIGURE 5 – THD+N VS. OUTPUT POWER**

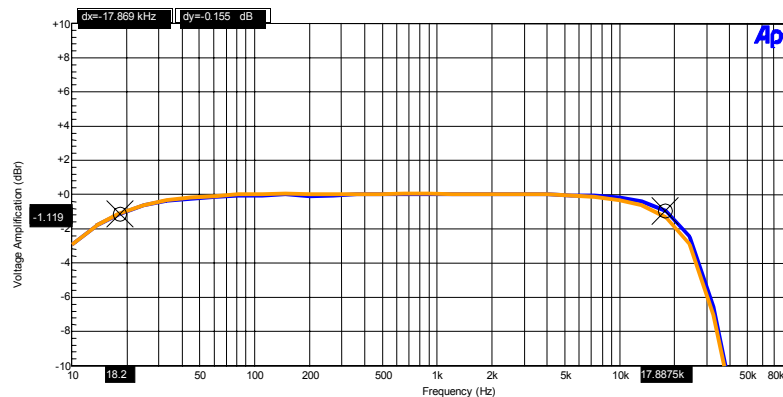
$V_{IN} = 25V$   
 $f_{IN} = 1kHz$   
 $R_L = 2\Omega$


**FIGURE 6 – THD+N VS. FREQUENCY**

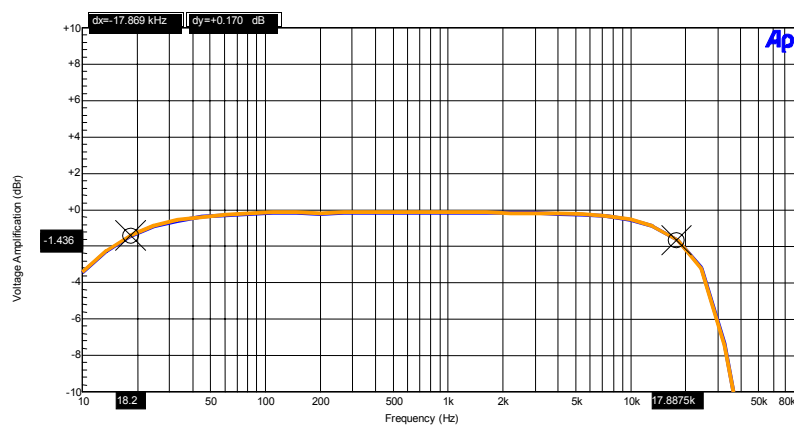
$V_{IN} = 15V$   
 $R_L = 4\Omega$   
 $P_O = 1W_{RMS}$


**FIGURE 7 – THD+N VS. FREQUENCY**

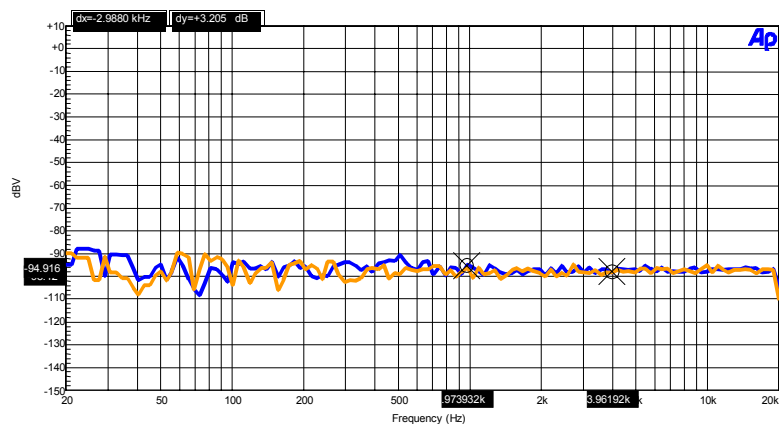
$V_{IN} = 25V$   
 $R_L = 4\Omega$   
 $P_O = 1W_{RMS}$

**CHARACTERISTIC CURVES (CONTINUED)**

**FIGURE 8 – FREQUENCY RESPONSE**

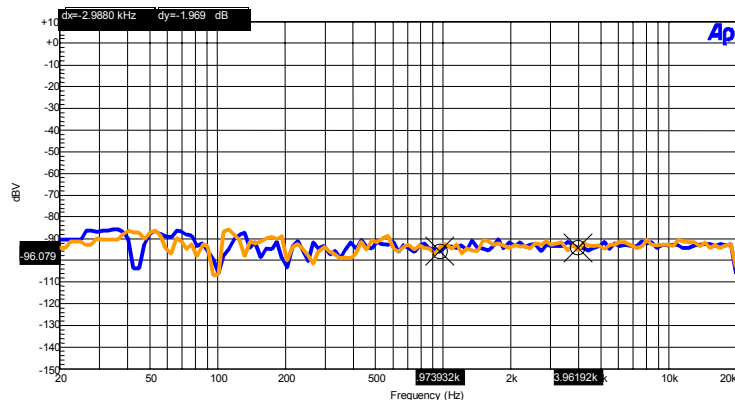
$V_{IN} = 15V$   
 $R_L = 4\Omega$   
 $P_O = 1W_{RMS}$


**FIGURE 9 – FREQUENCY RESPONSE**

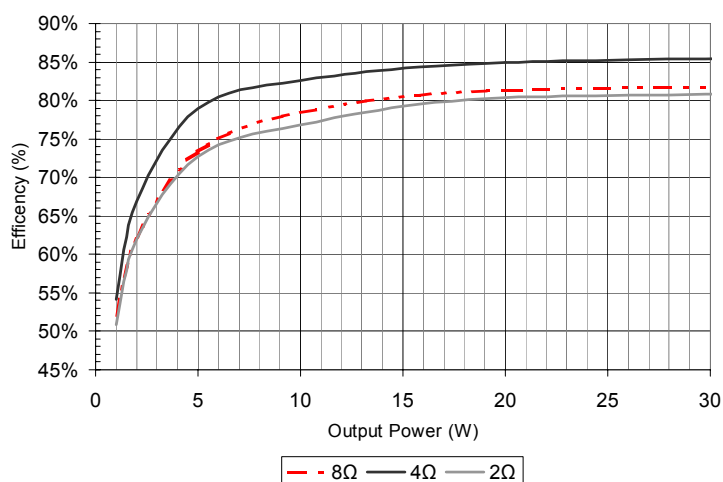
$V_{IN} = 25V$   
 $R_L = 4\Omega$   
 $P_O = 1W_{RMS}$


**FIGURE 10 – NOISE FLOOR FFT**

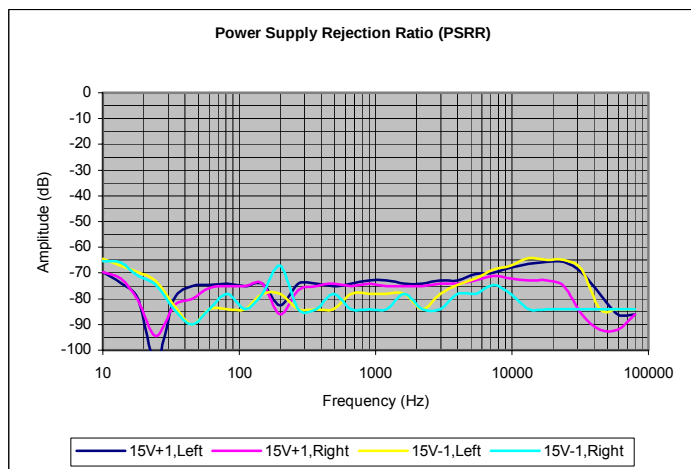
$V_{IN} = 15V$   
 $R_L = 4\Omega$   
 10Hz – 22kHz Bandwidth  
 A-weighted

**CHARACTERISTIC CURVES (CONTINUED)**

**FIGURE 11 – NOISE FLOOR FFT**

$V_{IN} = 25V$   
 $R_L = 4\Omega$   
 10Hz – 22kHz Bandwidth  
 A-Weighted


**FIGURE 12 – EFFICIENCY VS. OUTPUT POWER**

$V_{IN} = 15V$   
 $f_{IN} = 1kHz$


**FIGURE 13 – POWER SUPPLY REJECTION RATIO (PSSR)**

$P_O = 1W_{RMS}$   
 $R_L = 4\Omega$



APPLICATION

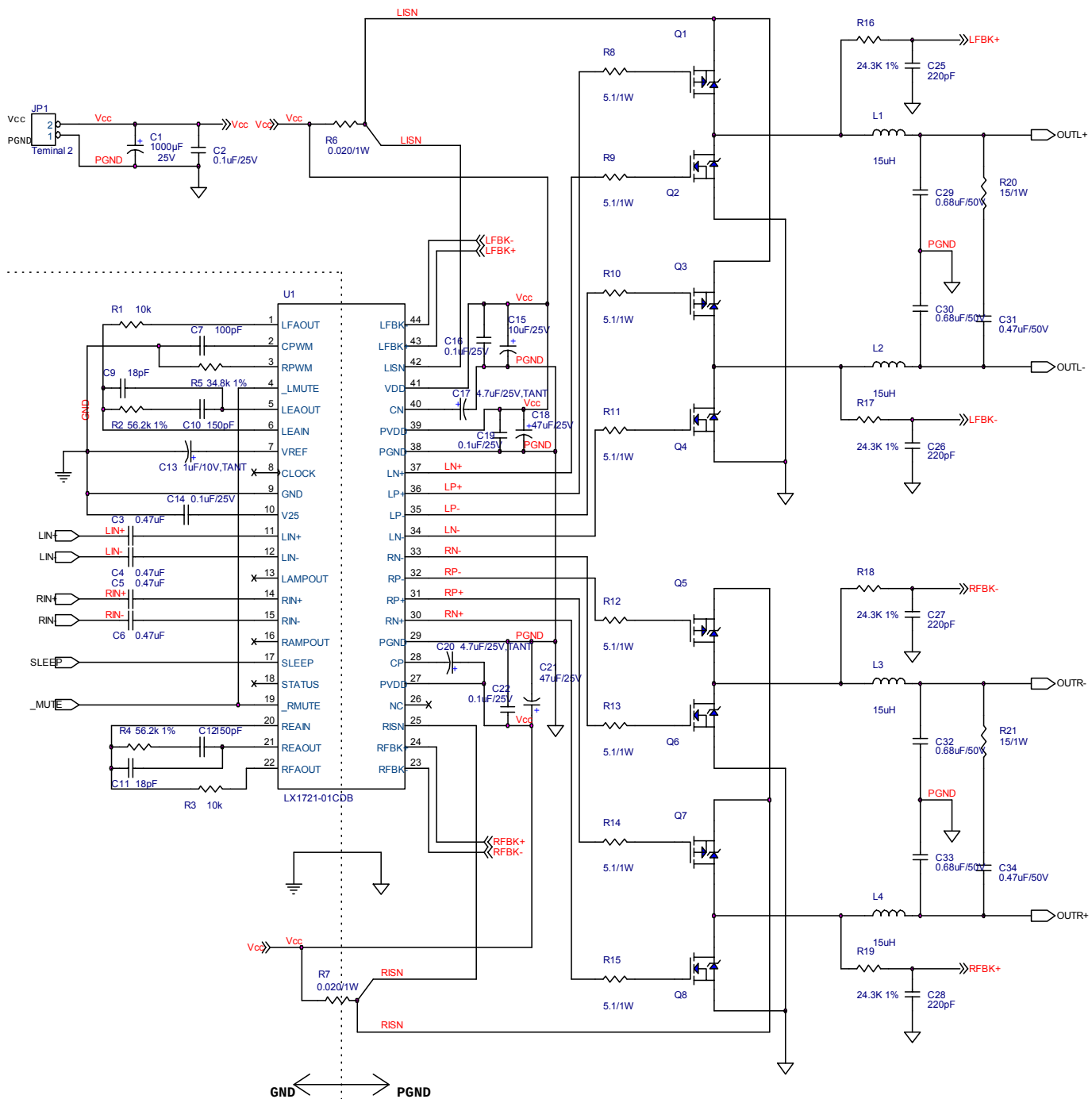
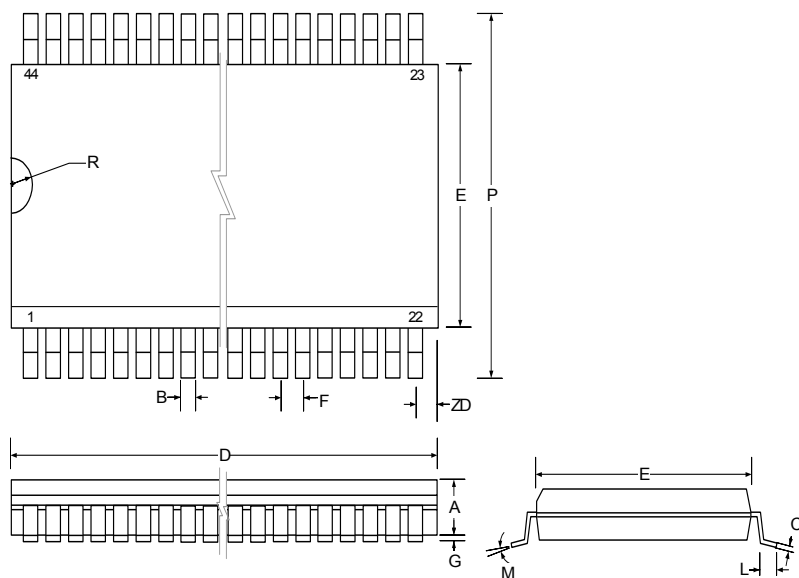


FIGURE 14 – TYPICAL CLASS-D STEREO SWITCHING AMPLIFIER CIRCUIT APPLICATION

**MECHANICAL DIMENSIONS**
**DB 44-Pin Quarter Size Outline Package (QSOP)**


| Dim | MILLIMETERS |       | INCHES     |        |
|-----|-------------|-------|------------|--------|
|     | MIN         | MAX   | MIN        | MAX    |
| A   | 2.44        | 2.64  | 0.096      | 0.104  |
| B   | 0.28        | 0.51  | 0.011      | 0.020  |
| C   | 0.23        | 0.32  | 0.091      | 0.0125 |
| D   | 17.73       | 17.93 | 0.698      | 0.706  |
| E   | 7.40        | 7.60  | 0.291      | 0.299  |
| F   | 0.80 BSC    |       | 0.0315 BSC |        |
| G   | 0.10        | 0.30  | 0.004      | 0.012  |
| L   | 0.40        | 1.27  | 0.016      | 0.050  |
| M   | 0°          | 8°    | 0°         | 8°     |
| P   | 10.11       | 10.51 | 0.396      | 0.414  |
| R   | 0.63        | 0.89  | 0.025      | 0.035  |
| ZD  | 0.51 REF    |       | 0.033 REF  |        |
| *LC | -           | 0.10  | -          | 0.004  |

\* Lead Coplanarity

**Note:** Dimensions do not include mold flash or protrusions; these shall not exceed 0.15mm (.006") on any side. Lead dimension shall not include solder coverage.

NOTES

PRODUCTION DATA – Information contained in this document is proprietary to Microsemi and is current as of publication date. This document may not be modified in any way without the express written consent of Microsemi. Product processing does not necessarily include testing of all parameters. Microsemi reserves the right to change the configuration and performance of the product and to discontinue product at any time.