

FSQ100

Green Mode Fairchild Power Switch (FPS™)

Features

- Internal Avalanche-Rugged SenseFET
- Precision Fixed Operating Frequency (67KHz)
- Burst-Mode Operation
- Internal Start-up Circuit
- Pulse-by-Pulse Current Limiting
- Over-Voltage Protection (OVP)
- Overload Protection (OLP)
- Internal Thermal Shutdown Function (TSD)
- Auto-Restart Mode
- Under-Voltage Lockout (UVLO) with Hysteresis
- Built-in Soft Start
- Secondary-Side Regulation

Applications

- Charger & Adapter for Mobile Phone, PDA, MP3
- Auxiliary Power for White Goods, PC, C-TV, Monitor

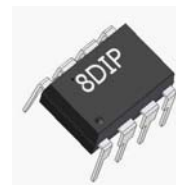
Related Application Notes

- *AN-4137 Design Guidelines for Off-line Flyback Converters using FPS™*
- *AN-4141 Troubleshooting and Design Tips for Fairchild Power Switch (FPS™) Flyback Applications*
- *AN-4147 Design Guidelines for RCD Snubber of Flyback*
- *AN-4134 Design Guidelines for Off-line Forward Converters using FPS™*
- *AN-4138 Design Considerations for Battery Charger Using Green Mode Fairchild Power Switch (FPS™)*

Description

The FSQ100 consists of an integrated Pulse Width Modulator (PWM) and SenseFET, specifically designed for high-performance, off-line, Switch-Mode Power Supplies (SMPS) with minimal external components. This device is an integrated high-voltage power switching regulator that combines a VDMOS SenseFET with a voltage mode PWM control block. The integrated PWM controller features include a fixed oscillator, Under-Voltage Lockout (UVLO) protection, Leading Edge Blanking (LEB), an optimized gate turn-on/turn-off driver, Thermal Shutdown (TSD) protection, and temperature-compensated precision-current sources for loop compensation and fault protection circuitry.

When compared to a discrete MOSFET and controller or RCC solution, the FSQ100 device reduces total component count and design size and weight, while increasing efficiency, productivity, and system reliability. This device provides a basic platform well suited for cost-effective flyback converters.



Ordering Information

Product Number	Package	Marking Code	BV _{DSS}	f _{osc}	R _{DS(ON)}
FSQ100	8-DIP	Q100	650V	67KHz	16Ω

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Pin Assignments

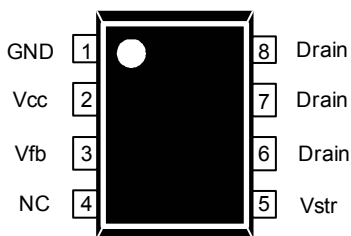


Figure 3. Pin Configuration (Top View)

Pin Definitions

Pin #	Name	Description
1	GND	Ground. SenseFET source terminal on primary side and internal control ground.
2	V _{cc}	Positive Supply Voltage Input. Although connected to an auxiliary transformer winding, current is supplied from pin 5 (V _{str}) via an internal switch during start-up (see Figure 2). When V _{CC} reaches the UVLO upper threshold (9V), the internal start-up switch opens and device power is supplied via the auxiliary transformer winding.
3	V _{fb}	Feedback. Inverting input to the PWM comparator with its normal input level lies between 0.5V and 2.5V. It has a 0.4mA current source connected internally, while a capacitor and opto-coupler are typically connected externally. A feedback voltage of 4.5V triggers overload protection (OLP). There is a time delay while charging external capacitor C _{fb} from 3V to 4.5V using an internal 5μA current source. This time delay prevents false triggering under transient conditions, but still allows the protection mechanism to operate in true overload conditions.
4	NC	No Connection.
5	V _{str}	Start-up. This pin connects directly to the rectified AC line voltage source. At start-up, the internal switch supplies internal bias and charges an external storage capacitor placed between the V _{CC} pin and ground. Once the V _{CC} reaches 9V, the internal switch stops charging the capacitor.
6,7,8	Drain	SenseFET Drain. The drain pins are designed to connect directly to the primary lead of the transformer and are capable of switching a maximum of 650V. Minimizing the length of the trace connecting these pins to the transformer decreases leakage inductance.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. $T_A = 25^\circ\text{C}$, unless otherwise specified.

Symbol	Parameter	Value	Unit
V_{DRAIN}	Drain Pin Voltage	650	V
V_{STR}	Vstr Pin Voltage	650	V
V_{DG}	Drain-Gate Voltage	650	V
V_{GS}	Gate-Source Voltage	± 20	V
V_{CC}	Supply Voltage	20	V
V_{FB}	Feedback Voltage Range	-0.3 to V_{STOP}	V
P_{D}	Total Power Dissipation	1.40	W
T_{J}	Operating Junction Temperature	Internally limited	$^\circ\text{C}$
T_{A}	Operating Ambient Temperature	-25 to +85	$^\circ\text{C}$
T_{STG}	Storage Temperature	-55 to +150	$^\circ\text{C}$

Notes:

1. Repetitive rating: Pulse width is limited by maximum junction temperature.
2. $L = 24\text{mH}$, starting $T_{\text{J}} = 25^\circ\text{C}$.

Thermal Impedance

$T_A = 25^\circ\text{C}$, unless otherwise specified. All items are tested with the JEDEC standards JESD 51-2 and 51-10 (DIP).

Symbol	Parameter	Value	Unit
θ_{JA}	Junction-to-Ambient Thermal Impedance ⁽³⁾	88.84	$^\circ\text{C/W}$
θ_{JC}	Junction-to-Case Thermal Impedance ⁽⁴⁾	13.94	$^\circ\text{C/W}$

Notes:

3. Free-standing with no heatsink; without copper clad. Measurement condition – just before junction temperature T_{J} enters into OTP.
4. Measured on the DRAIN pin close to plastic interface.

Electrical Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SenseFET Section						
I _{DSS}	Zero-Gate-Voltage Drain Current	V _{DS} =650V, V _{GS} =0V			25	μA
		V _{DS} =520V, V _{GS} =0V, T _C =125°C			200	
R _{DS(ON)}	Drain-Source On-State Resistance ⁽⁵⁾	V _{GS} =10V, I _D =0.5A		16	22	Ω
g _{fs}	Forward Trans-Conductance	V _{DS} =50V, I _D =0.5A	1.0	1.3		S
C _{ISS}	Input Capacitance	V _{GS} =0V, V _{DS} =25V, f=1MHz		162		pF
C _{OSS}	Output Capacitance			18		
C _{RSS}	Reverse Transfer Capacitance			3.8		
Control Section						
f _{OSC}	Switching Frequency		61	67	73	kHz
Δf _{OSC}	Switching Frequency Variation ⁽⁶⁾	-25°C ≤ T _A ≤ 85°C		±5	±10	%
D _{MAX}	Maximum Duty Cycle		60	67	74	%
V _{START}	UVLO Threshold Voltage	V _{FB} =GND	8	9	10	V
V _{STOP}		V _{FB} =GND	6	7	8	V
I _{FB}	Feedback Source Current	0V ≤ V _{FB} ≤ 3V	0.35	0.40	0.45	mA
t _{S/S}	Internal Soft Start Time		10	15	20	ms
Burst Mode Section						
V _{BURH}	Burst Mode Voltage	T _J =25°C	0.6	0.7	0.8	V
V _{BURL}			0.45	0.55	0.65	V
V _{BUR(HYS)}		Hysteresis		150		mV
Protection Section						
I _{LIM}	Peak Current Limit		0.475	0.550	0.650	A
T _{SD}	Thermal Shutdown Temperature ⁽⁷⁾		125	145		°C
V _{SD}	Shutdown Feedback Voltage		4.0	4.5	5.0	V
V _{OV}	Over-Voltage Protection		20			V
I _{DELAY}	Shutdown Delay Current	3V ≤ V _{FB} ≤ V _{SD}	4	5	6	μA
Total Device Section						
I _{OP}	Operating Supply Current ⁽⁸⁾	V _{CC} ≤ 16V		1.5	3.0	mA
I _{CH}	Start-Up Charging Current	V _{CC} =0V, V _{STR} =50V	450	550	650	μA

Notes:

5. Pulse test: Pulse width ≤ 300μs, duty ≤ 2%.
6. These parameters, although guaranteed, are tested in EDS (wafer test) process.
7. These parameters, although guaranteed, are not 100% tested in production.
8. Control part only.

Typical Performance Characteristics

These characteristic graphs are normalized at $T_A = 25^\circ\text{C}$.

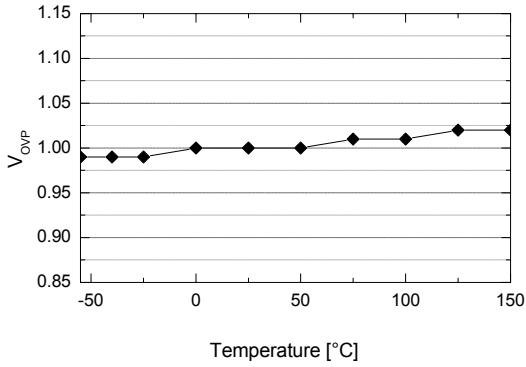


Figure 4. Over-Voltage Protection (V_{OVP}) vs. T_A

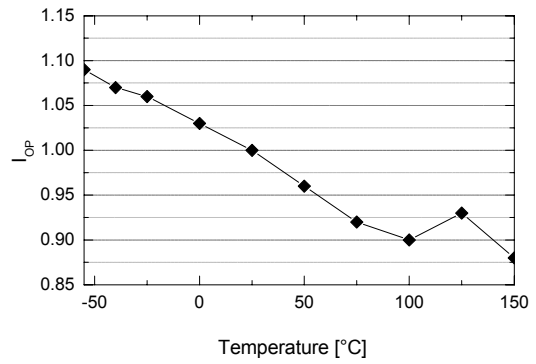


Figure 5. Operating Supply Current (I_{OP}) vs. T_A

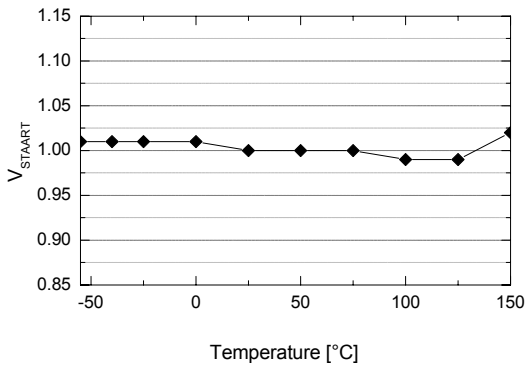


Figure 6. Start Threshold Voltage (V_{START}) vs. T_A

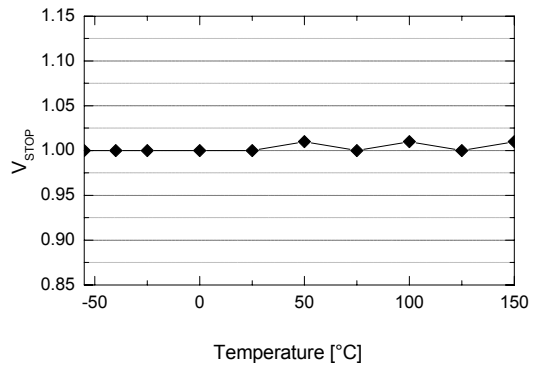


Figure 7. Stop Threshold Voltage (V_{STOP}) vs. T_A

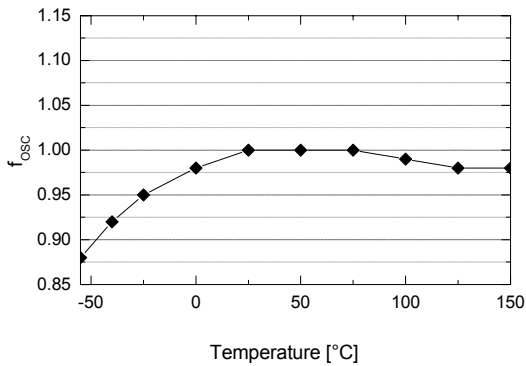


Figure 8. Operating Frequency (f_{OSC}) vs. T_A

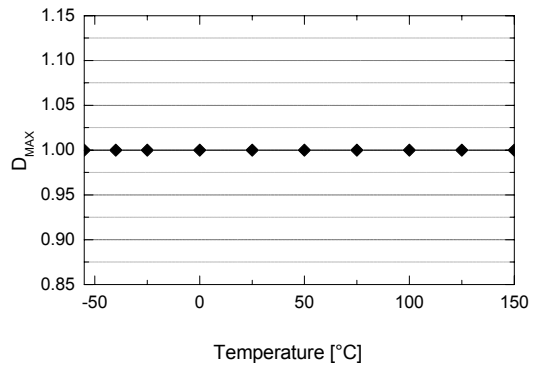


Figure 9. Maximum Duty Cycle (D_{MAX}) vs. T_A

Typical Performance Characteristics (Continued)

These characteristic graphs are normalized at $T_A = 25^\circ\text{C}$.

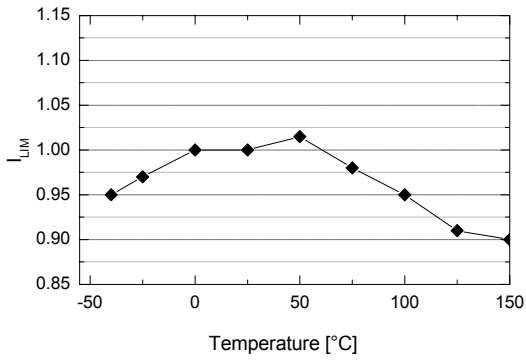


Figure 10. Peak Current Limit (I_{LIM}) vs. T_A

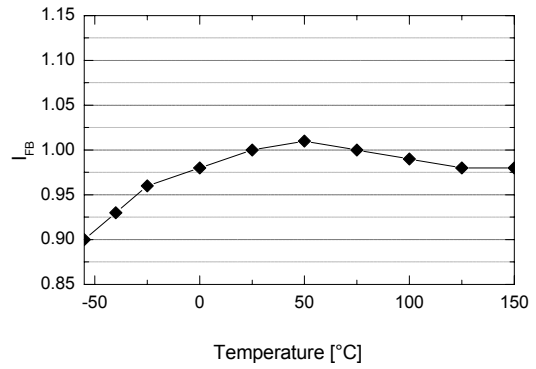


Figure 11. Feedback Source Current (I_{FB}) vs. T_A

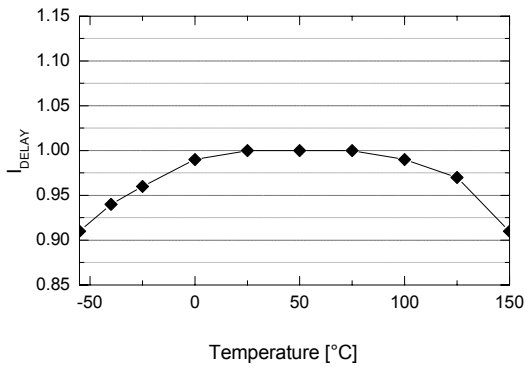


Figure 12. Shutdown Delay Current (I_{DELAY}) vs. T_A

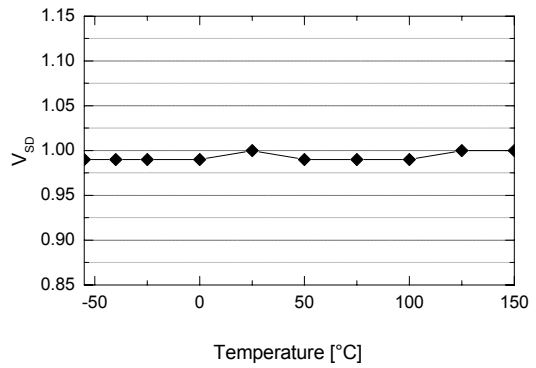


Figure 13. Shutdown Feedback Voltage (V_{SD}) vs. T_A

Functional Description

1. Start-up: At start-up, the internal high-voltage current source supplies the internal bias and charges the external V_{CC} capacitor, as shown in Figure 14. When V_{CC} reaches 9V, the device starts switching and the internal high-voltage current source stops charging the capacitor. The device is in normal operation provided V_{CC} does not drop below 7V. After start-up, the bias is supplied from the auxiliary transformer winding.

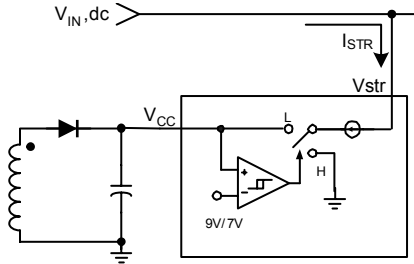


Figure 14. Internal Start-up Circuit

Calculating the V_{CC} capacitor is an important step to design with the FSQ100. At initial start-up, the maximum value of start operating current I_{START} is about $100\mu A$, which supplies current to UVLO and V_{REF} blocks. The charging current I_{VCC} of the V_{CC} capacitor is equal to $I_{STR} - 100\mu A$. After V_{CC} reaches the UVLO start voltage, only the bias winding supplies V_{CC} current to the device. When the bias winding voltage is not sufficient, the V_{CC} level decreases to the UVLO stop voltage and the internal current source is activated again to charge the V_{CC} capacitor. To prevent this V_{CC} fluctuation (charging/discharging), the V_{CC} capacitor should be chosen to have a value between $10\mu F$ and $47\mu F$.

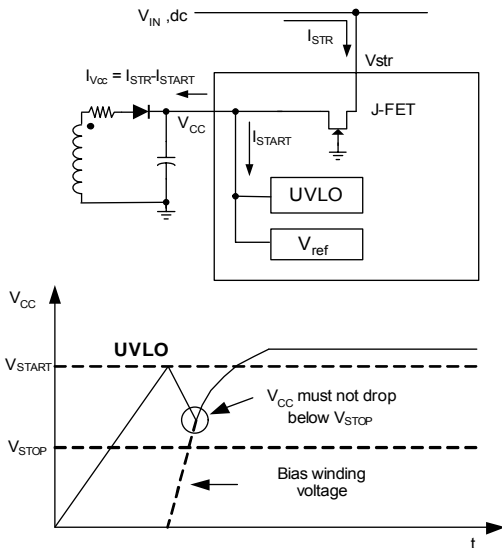


Figure 15. Charging V_{CC} Capacitor through V_{str}

2. Feedback Control: The FSQ100 is a voltage mode controlled device, as shown in Figure 16. Usually, an opto-coupler and shunt regulator, like KA431 are used to implement the feedback network. The feedback voltage is compared with an internally generated sawtooth waveform. This directly controls the duty cycle.

When the shunt regulator reference pin voltage exceeds the internal reference voltage of 2.5V, the opto-coupler LED current increases, the feedback voltage V_{FB} is pulled down, and it reduces the duty cycle. This happens when the input voltage increases or the output load decreases.

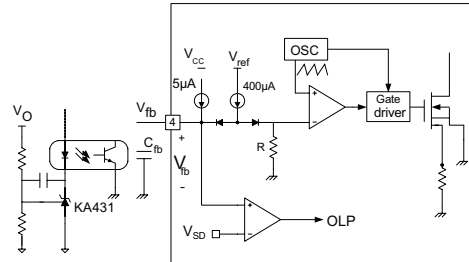


Figure 16. PWM and Feedback Circuit

3. Leading Edge Blanking (LEB): At the instant the internal SenseFET is turned on, the primary-side capacitance and secondary-side rectifier diode reverse recovery typically causes a high-current spike through the SenseFET. Excessive voltage across the R_{SENSE} resistor lead to incorrect pulse-by-pulse current limit protection. To avoid this, a leading edge blanking (LEB) circuit disables pulse-by-pulse current-limit protection block for a fixed time (t_{LEB}) after the SenseFET turns on.

4. Protection Circuit: The FSQ100 has protective functions, such as overload protection (OLP), over voltage protection (OVP), under-voltage lockout (UVLO), and thermal shutdown (TSD). Because these protection circuits are fully integrated inside the IC without external components, reliability is improved without increasing costs. Once a fault condition occurs, switching is terminated and the SenseFET remains off. This causes V_{CC} to fall. When V_{CC} reaches the UVLO stop voltage V_{STOP} (7V), the protection is reset and the internal high-voltage current source charges the V_{CC} capacitor via the V_{str} pin. When V_{CC} reaches the UVLO start voltage V_{START} (9V), the device resumes normal operation. In this manner, the auto-restart can alternately enable and disable the switching of the power SenseFET until the fault condition is eliminated.

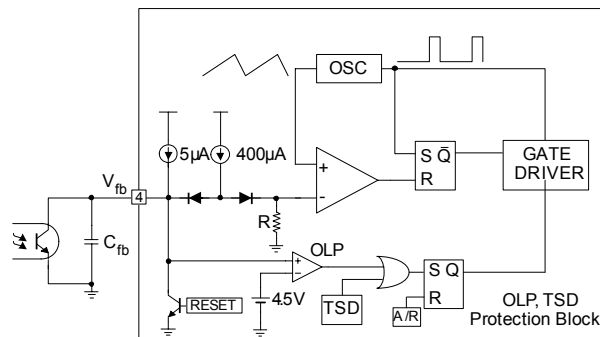
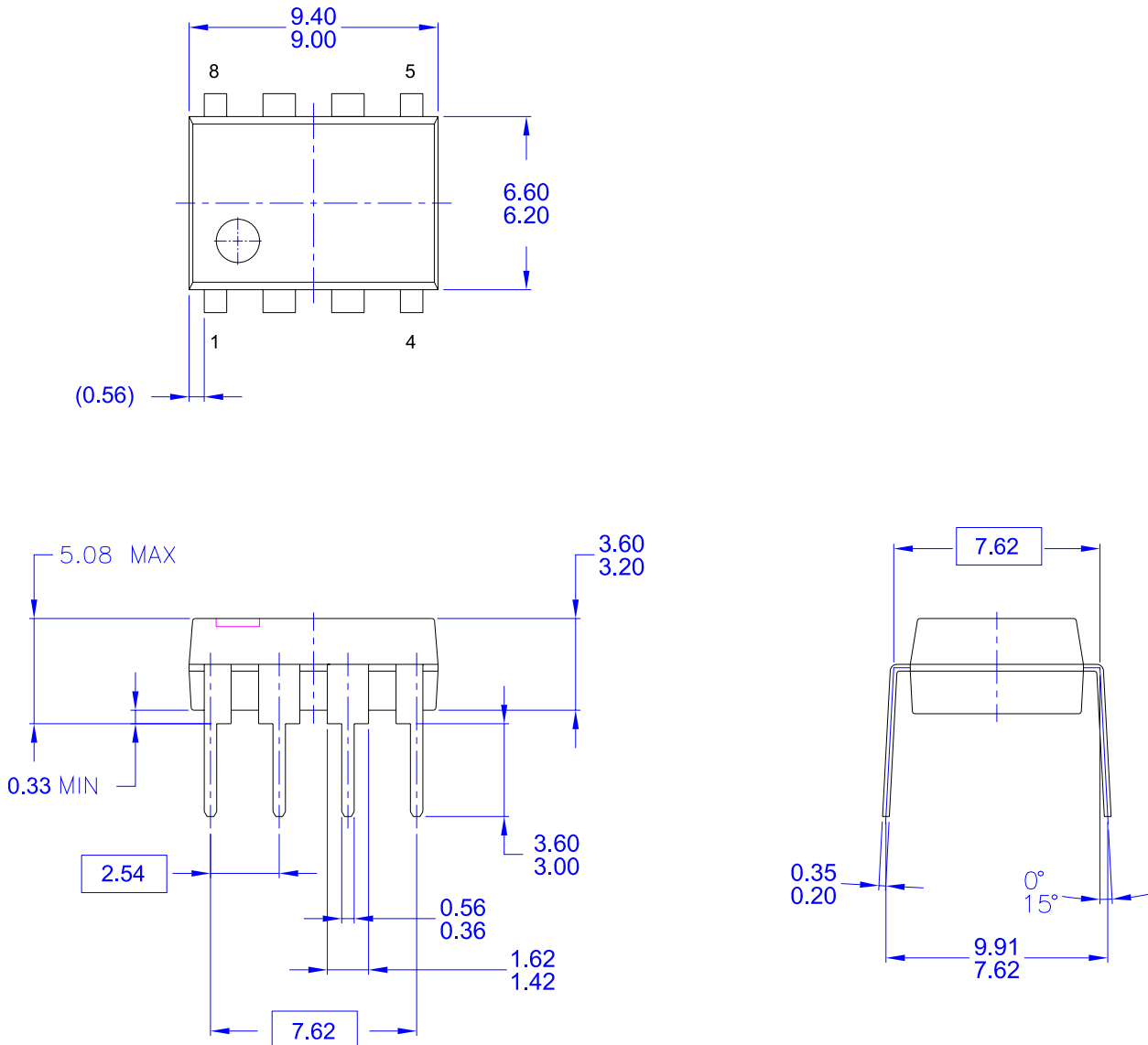


Figure 17. Protection Block

Physical Dimensions

Dimensions are in millimeters and inches unless otherwise noted.



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC MS-001 VARIATION BA
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D) DIMENSIONS AND TOLERANCES PER ASME Y14.5 M-1994

MKT-N08FrevA

Figure 24. 8-Pin Dual In Line Package (DIP)

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