2x25W Stereo / 1x50W Mono Digital Audio Amplifier With 32 bands EQ and DRC Functions

Features

- 16/18/20/24-bits input with I^2S, Left-alignment, Right-alignment and TDM data format
- PSNR & DR(A-weighting)
  Loudspeaker: 107dB (PSNR), 108dB (DR)@24V
- Multiple sampling frequencies (Fs)
  8kHz, 16kHz, 32kHz/44.1kHz/48kHz and 64kHz/88.2kHz/96kHz
- System clock = 64x, 128x, 192x, 256x, 384x, 512x, 576x, 768x, 1024x Fs
  MCLK system: (option with AD82129)
  256x~4096x Fs for 8kHz
  128x~2048x Fs for 16kHz
  64x~1024x Fs for 32kHz/44.1kHz/48kHz
  64x~512x Fs for 64kHz/88.2kHz/96kHz
  BCLK system:
  256x Fs for 8kHz (TDM mode)
  128x Fs and 256xFs for 16kHz (TDM mode)
  64x Fs for 32kHz/44.1kHz/48kHz
  64x Fs for 64kHz/88.2kHz/96kHz
- Supply voltage
  1.65~3.6V for DVDDIO (option with AD82121)
  3.0~3.6V for DVDD
  4.5~26V for PVDD
- Supports 2.0CH/Mono configuration
- Loudspeaker output power@12V for stereo
  8W x 2CH into 8Ω @ 1% THD+N
  15W x 2CH into 4Ω @ 1% THD+N
- Loudspeaker output power@24V for stereo
  25W x 2CH into 8Ω <1% THD+N
- Sound processing including：
  32 bands parametric speaker EQ
  Volume control (+24dB~-103dB, 0.125dB/step)
  Dynamic range control
  Three Band plus post Dynamic range control
  Power Clipping
  Programmed 3D surround sound
  Channel mixing
  Noise gate with hysteresis window
  DC-blocking high-pass filter
  Pre-scale/post-scale
  Post-Boost (+48dB)
  I2S output with user programmed gain (+24dB~mute)
- Anti-pop design
- Level meter and power meter
- I^2S output with selectable Audio DSP point
- Short circuit and over-temperature protection
- Supports I^2C control without clock
- I^2C control interface with selectable device address
- Support hardware and software reset
- Internal PLL
- LV Under-voltage shutdown and HV Under-voltage detection
- Over voltage protection

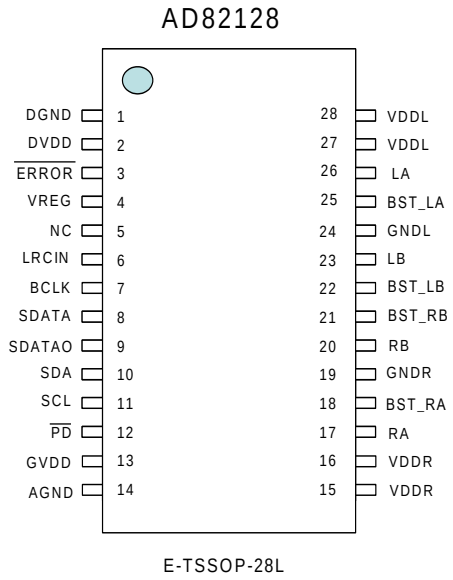
Applications

- TV audio
- Boom-box, CD and DVD receiver, docking system
- Powered speaker
- Wireless audio

Description

AD82128 is a digital audio amplifier capable of driving 25W (BTL) each to a pair of 8Ω load speaker and 50W (PBTL) to a 4Ω load speaker operating at 24V supply without external heat-sink or fan requirement with play music. AD82128 provides advanced audio processing functions, such as volume control, 32 EQ bands, audio mixing, 3D surround sound and Dynamic Range Control (DRC). These are fully programmable via a simple I^2C control interface. Robust protection circuits are provided to protect AD82128 from damage due to accidental erroneous operating condition. The full digital circuit design of AD82128 is more tolerant to noise and PVT (Process, Voltage, and Temperature) variation than the analog class-AB or class-D audio amplifier counterpart implemented by analog circuit design. AD82128 is pop free during instantaneous power on/off or mute/shut down switching because of its robust built-in anti-pop circuit.

Pin Assignment



E-TSSOP-28L

Pin Description

PIN	NAME	TYPE	DESCRIPTION	CHARACTERISTICS
1	DGND	P	Digital Ground.	
2	DVDD	P	Digital Power.	
3	$\overline{\text{ERROR}}$	AI/O	This Pin is a dual function pin. One is I2C address setting during power up initial. After power up, it is indicator for error status report (low active), it sets by register of A_SEL_FAULT at address 0x1C B[6] to enable it.	This pin is monitored on the rising edge of reset. It will determine the slave address of AD82128 and define in the device addressing part.
4	VREG	P	1.8V Regulator voltage output, this pin must not be used to drive external devices.	
5	NC		Not connected.	
6	LRCIN	DI	Left/Right clock input (Fs).	Schmitt trigger TTL input buffer, internal pull Low with a 100Kohm resistor.
7	BCLK	DI	Bit clock input.	Schmitt trigger TTL input buffer, internal pull Low with a 100Kohm resistor.
8	SDATA	DI	Serial audio data input.	Schmitt trigger TTL input buffer
9	SDATAO	DO	Serial audio data output.	Schmitt trigger TTL input buffer

10	SDA	DI/O	I^2C bi-directional serial data.	Schmitt trigger TTL input buffer
11	SCL	DI	I^2C serial clock input.	Schmitt trigger TTL input buffer
12	$\overline{PD}$	AI	Power down, low active. Place the amplifier in Shutdown.	Schmitt trigger TTL input buffer, internal pull Low with a 100Kohm resistor.
13	GVDD	P	5V Regulator voltage output, this pin must not be used to drive external devices.	
14	AGND	P	Analog Ground.	
15	VDDR	P	Right channel supply.	
16	VDDR	P	Right channel supply.	
17	RA	O	Right channel output A.	
18	BST_RA	P	Bootstrap capacitor connect pin for right channel output A, it is used to create a power supply for the high-side gate drive for right channel output A.	
19	GNDR	P	Right channel ground.	
20	RB	O	Right channel output B.	
21	BST_RB	P	Bootstrap capacitor connect pin for right channel output B, it is used to create a power supply for the high-side gate drive for right channel output B.	
22	BST_LB	P	Bootstrap capacitor connect pin for left channel output B, it is used to create a power supply for the high-side gate drive for left channel output B.	
23	LB	O	Left channel output B.	
24	GNDL	P	Left channel ground.	
25	BST_LA	P	Bootstrap capacitor connect pin for left channel output A, it is used to create a power supply for the high-side gate drive for left channel output A.	
26	LA	O	Left channel output A.	
27	VDDL	P	Left channel supply.	
28	VDDL	P	Left channel supply.	
Thermal land			Connect to the system ground.	